Mobile SDRAM

MT48H32M16LF – 8 Meg x 16 x 4 banks
MT48H16M32LF/LG – 4 Meg x 32 x 4 banks

Features

- Endur-IC™ technology
- Fully synchronous; all signals registered on positive edge of system clock
- VDD = 1.7–1.95V; VDDQ = 1.7–1.95V
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable burst lengths: 1, 2, 4, 8, and continuous[1]
- Auto precharge, includes concurrent auto precharge
- Auto refresh and self refresh modes
- LVTTL-compatible inputs and outputs
- On-chip temperature sensor to control refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive (DS)

Table 1: Configuration Addressing

DQ Bus Width	Architecture	JEDEC-Standard Option	Reduced Page-Size Option[2]
	Number of banks	4	4
	Bank address balls	BA0, BA1	BA0, BA1
x16	Row address balls	A0–A12	–
	Column address balls	A0–A9	–
x32	Row address balls	A0–A12	A0–A13
	Column address balls	A0–A8	A0–A7

Table 2: Key Timing Parameters
CL = CAS (READ) latency

Speed Grade	Clock Rate (MHz)		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-75	104	133	9ns	6ns
-8	100	125	9ns	7ns

Options — Marking

Options	Marking
• VDD/VDDQ	
– 1.8V/1.8V	H
• Row size option	
– Standard addressing option	LF
– Reduced page-size option	LG[3, 4]
• Configuration	
– 32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
– 16 Meg x 32 (4 Meg x 32 x 4 banks)	16M32
• Plastic “green” packages	
– 54-Ball VFBGA (10mm x 11.5mm)	CJ[5]
– 90-Ball VFBGA (10mm x 13mm)	CM[3]
• Timing – cycle time	
– 7.5ns at CL = 3	-75
– 8ns at CL = 3	-8
• Power	
– Standard IDD2P/IDD7	None
– Low IDD2P/IDD7	L
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
• Design revision	:A

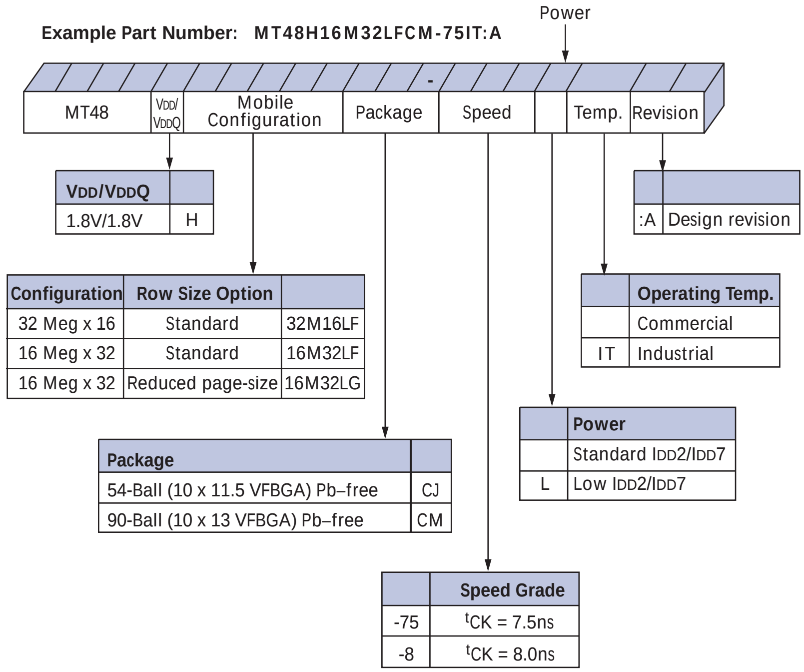
Notes:
1. For continuous page burst, contact factory for availability.
2. For reduced page-size option, contact factory for availability.
3. LG is a reduced page-size option. Contact factory for availability.
4. Only available for x32 configuration.
5. Only available for x16 configuration.

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Figure 1: 512Mb Mobile SDRAM Part Numbering



VDD/VDDQ	
1.8V/1.8V	H

Configuration	Row Size Option	
32 Meg x 16	Standard	32M16LF
16 Meg x 32	Standard	16M32LF
16 Meg x 32	Reduced page-size	16M32LG

Package	
54-Ball (10 x 11.5 VFBGA) Pb–free	CJ
90-Ball (10 x 13 VFBGA) Pb–free	CM

	Speed Grade
-75	^{t}CK = 7.5ns
-8	^{t}CK = 8.0ns

	Power
	Standard IDD2/IDD7
L	Low IDD2/IDD7

	Operating Temp.
	Commercial
IT	Industrial

:A	Design revision

General Description

The Micron® 512Mb Mobile SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1K columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits. In a reduced page-size option, each of the x32's 134,217,728-bit banks is organized as 16,384 rows by 256 columns x32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations with a read burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

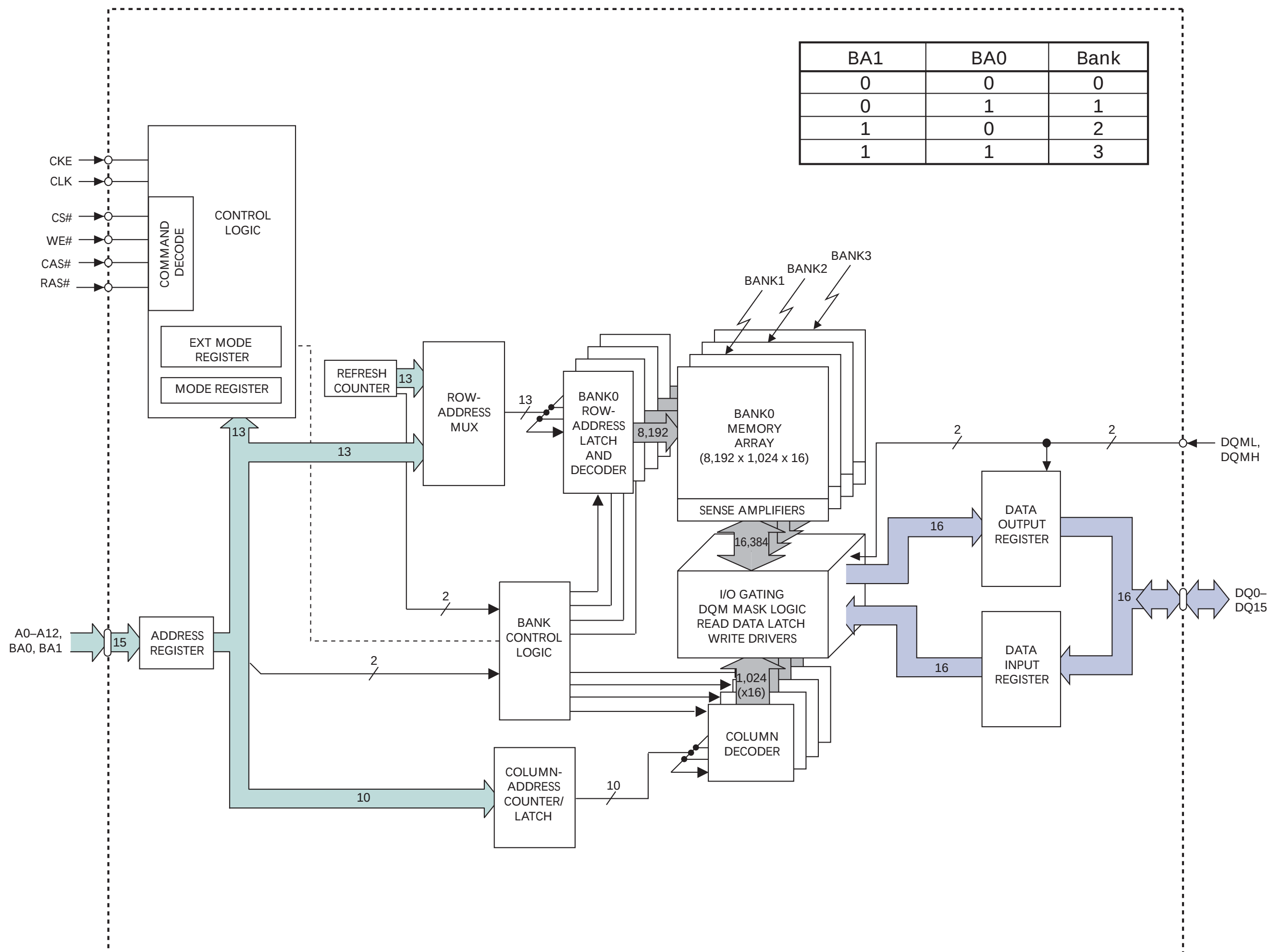
The 512Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless high-speed, random-access operation.

The 512Mb SDRAM is designed to operate in 1.8V low-power memory systems. An auto refresh mode is provided, along with a power-saving deep power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

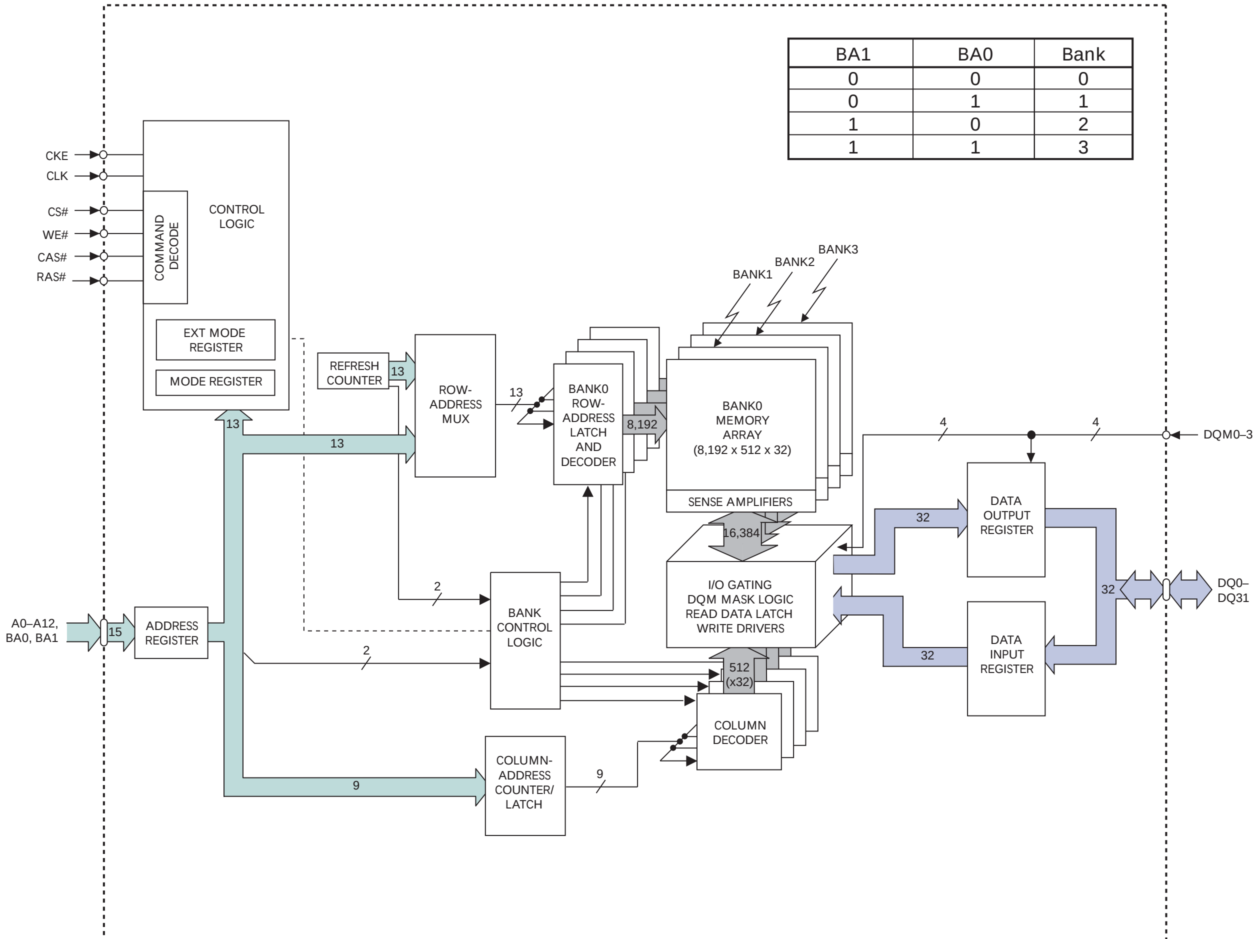
Functional Block Diagrams

Figure 2: 32 Meg x 16 SDRAM



BA1	BA0	Bank
0	0	0
0	1	1
1	0	2
1	1	3

Figure 3: 16 Meg x 32 SDRAM



BA1	BA0	Bank
0	0	0
0	1	1
1	0	2
1	1	3

Ball Assignments

Figure 4: 54-Ball FBGA (Top View) – 10mm x 11.5mm

	1	2	3	4	5	6	7	8	9
A	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ				VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ				VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ				VSSQ	DQ6	DQ5
E	DQ8	VSSQ[1]	VSS				VDD	LDQM	DQ7
F	UDQM	CLK	CKE				CAS#	RAS#	WE#
G	A12	A11	A9				BA0	BA1	CS#
H	A8	A7	A6				A0	A1	A10
J	VSS	A5	A4				A3	A2	VDD

Notes: 1. The E2 pin is a test pin and must be tied to VSSQ in normal operation.

Figure 5: 90-Ball VFBGA (Top View) – 10mm x 13mm

	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	VSS				VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ				VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25				DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30				DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC				NC	DQ16	VSSQ
F	VSS	DQM3	A3				A2	DQM2	VDD
G	A4	A5	A6				A10	A0	A1
H	A7	A8	A12				A13/NC	BA1	A11
J	CLK	CKE	A9				BA0	CS#	RAS#
K	DQM1	DNU[1]	NC				CAS#	WE#	DQM0
L	VDDQ	DQ8	VSS				VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9				DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14				DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ				VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS				VDD	DQ0	DQ2

Notes: 1. The K2 “DNU” ball should not be used in the application. However, it may be connected to VSS (ground).

Ball Descriptions

Table 3: VFBGA Ball Descriptions

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
F2	J1	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	J2	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
G9	J8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F7, F8, F9	J9, K7, K8	CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
E8, F1	K9, K1, F8, F2	DQM0–3, LDQM, UDQM	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. For the x16, LDQM corresponds to DQ0–DQ7 and HDQM corresponds to DQ8–DQ16. For the x32, DQM0 corresponds to DQ0–DQ7, DQM1 corresponds to DQ8–DQ15, DQM2 corresponds to DQ16–DQ23, and DQM3 corresponds to DQ24–DQ31. DQM0–3 (or LDQM and HDQM if x16) are considered same state when referenced as DQM.
G7, G8	J7, H8	BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 become "don't care" when registering an ALL BANK PRECHARGE (A10 HIGH).
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2, G1	G8, G9, F7, F3, G1, G2, G3, H1, H2, J3, G7, H9, H3	A0–A12	Input	Address inputs: A0–A12 are sampled during the ACTIVE command (row-address A0–A12) and READ/WRITE command [column-address A0–A8 (x32); column-address A0–A9 (x16); with A10 defining auto precharge] to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command.
–	H7	A13/NC	Input	H7 is used for the LG, reduced page-size, option (see Table 1 on page 1); otherwise, leave as NC.

Table 3: VFBGA Ball Descriptions (Continued)

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	R8, N7, R9, N8, P9, M8, M7, L8, L2, M3, M2, P1, N2, R1, N3, R2, E8, D7, D8, B9, C8, A9, C7, A8, A2, C3, A1, C2, B1, D2, D3, E2	DQ0–DQ31	I/O	Data input/output: Data bus.
A7, B3, C7, D3	B2, B7, C9, D9, E1, L1, M9, N9, P2, P7	VDDQ	Supply	DQ power: Provide isolated power to DQ for improved noise immunity.
A3, B7, C3, D7	B8, B3, C1, D1, E9, L9, M1, N1, P3, P8	VSSQ	Supply	DQ ground: Provide isolated ground to DQ for improved noise immunity.
A9, E7, J9	A7, F9, L7, R7	VDD	Supply	Core power supply.
A1, E3, J1	A3, F1, L3, R3	VSS	Supply	Ground.
–	E3, E7, K3	NC	–	Internally not connected: These balls could be left unconnected, but it is recommended they be connected to VSS.
E2	–	VSSQ	–	This TEST pin must be tied to VSS or VSSQ in normal operation.
–	K2	DNU	–	Should not be used in the application. However, it may be connected to VSS (ground).

Functional Description

In general, the 512Mb SDRAMs (4 Meg x 32 x 4 banks) are quad-bank DRAMs that operate at 1.8V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK).

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0–A12 select the row). The address bits (A0–A9 for x16 and A0–A8 for x32) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once the power is applied to VDD and VDDQ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command must be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for programming the mode registers. Because the mode registers will power up in an unknown state, they should be loaded prior to applying any operational command.

Register Definition

Mode Register

There are two mode registers in the component: mode register and extended mode register (EMR). The mode register is illustrated in Figure 6 on page 14. The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length (BL), a burst type, a CAS latency (CL), an operating mode and a write burst mode, as shown in Figure 6 on page 14. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the BL, M3 specifies the type of burst, M4–M6 specify the CL, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 should be set to zero. M12 and M13 should be set to zero to prevent the extended mode register from being programmed.

The mode registers must be loaded when all banks are idle, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented, with the BL being programmable, as shown in Figure 6 on page 14. The BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. BL = 1, 2, 4, 8, or continuous locations are available for both the sequential and the interleaved burst types, and a continuous-page burst is available for the sequential type. The continuous-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary BLs.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

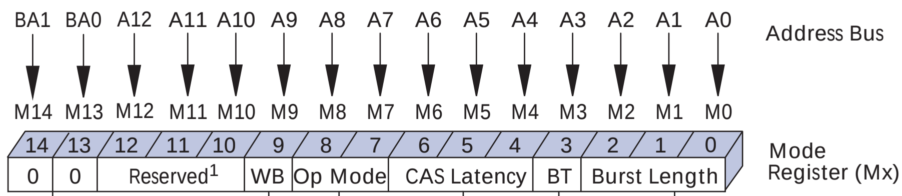
When a READ or WRITE command is issued, a block of columns equal to the BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A8 when BL = 2, A2–A8 when BL = 4, and A3–A8 when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the BL, the burst type, and the starting column address, as shown in Table 4 on page 15.

Figure 6: Mode Register Definition



M14	M13	Mode Register Definition
0	0	Base mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

M9	Write Burst Mode
0	Programmed burst length
1	Single location access

M8	M7	Operating Mode
0	0	Normal operation
–	–	All other states reserved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Notes: 1. Should be programmed to “0” to ensure compatibility with future devices.

Table 4: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

CAS Latency (CL)

The CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge $n + m$. The DQs will start driving as a result of the clock edge one cycle earlier ($n + m - 1$), and provided that the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 7 on page 16.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use.

Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

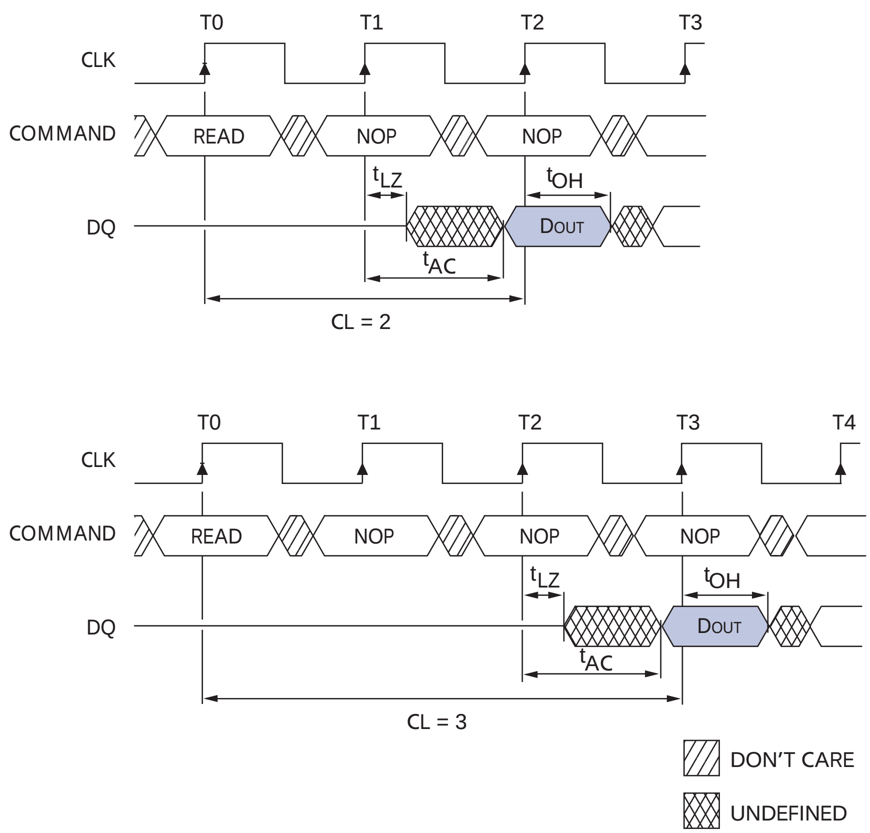
When M9 = 0, the BL programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed BL applies to READ bursts, but write accesses are single-location accesses.

Extended Mode Register (EMR)

The EMR controls the functions beyond those controlled by the mode register. These additional functions are special features of the mobile device that helps reduce overall system power consumption. They include temperature-compensated self refresh (TCSR) control, partial-array self refresh (PASR), and output drive strength.

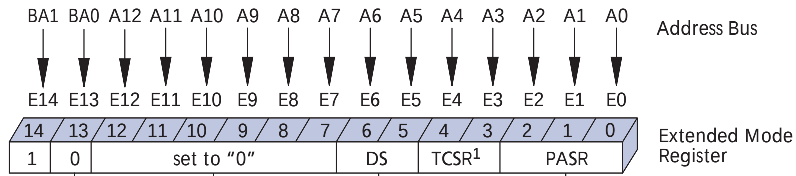
The EMR is programmed via the MODE REGISTER SET command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

Figure 7: CAS Latency



Notes:
1. Each READ command may be to any bank. DQM is LOW.
2. For CL = 2, DQM should be taken LOW at READ command. For CL = 3, DQM should be taken LOW one cycle after the READ command.

Figure 8: EMR Definition



E14	E13	Mode Register Definintion
0	0	Standard mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

E6	E5	Driver Strength
0	0	Full-strength driver
0	1	Half-strength driver
1	0	Quarter-strength driver
1	1	One eighth-strength driver

E12	E11	E10	E9	E8	E7	
0	0	0	0	0	0	Normal operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array
0	0	1	Half array
0	1	0	Quarter array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array
1	1	0	One-sixteenth array
1	1	1	Reserved

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

The extended mode register must be programmed with E7 through E12 set to "0." It must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. Once the values are entered, the extended mode register settings will be retained even after exiting deep power-down mode.

Temperature-Compensated Self Refresh (TCSR)

On this version of the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator. Programming of the TCSR bits will have no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the partial-array self refresh (PASR) feature allows the controller to select the amount of memory that will be refreshed during self refresh. The following refresh options are available.

1. All banks (banks 0, 1, 2, and 3).
2. Two banks (banks 0 and 1; BA1=0).
3. One bank (bank 0; BA1 = BA0 = 0).
4. Half bank (bank 0; BA1 = BA0 = row address MSB = 0).
5. Quarter bank (bank 0; BA1 = BA0; row address MSB = row address MSB - 1 = 0).

WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks or segments of a bank in PASR will be refreshed during self refresh. It is important to note that data in unused banks or portions of banks will be lost when PASR is used.

Driver Strength

Bits E5 and E6 of the extended mode register can be used to select the driver strength of the DQ outputs. This value should be set according to the application's requirements.

Commands

Table 5 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear on pages 41–44; these tables provide current state/next state information.

Table 5: Truth Table – Commands and DQM Operation
Notes 4 and 5 apply to all commands

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	1
NO OPERATION (NOP)	L	H	H	H	X	X	X	1
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	2
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/Col	X	3
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/Col	Valid	3
BURST TERMINATE or deep power-down (Enter deep power-down mode)	L	H	H	L	X	X	X	6, 7, 8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	9
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	10, 11
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	12
Write enable/output enable	X	X	X	X	L	X	Active	
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	

Notes:
1. COMMAND INHIBIT and NOP are functionally interchangeable.
2. BA0–BA1 provide bank address and A0–A12 provide row address.
3. BA0–BA1 provide bank address; A0–A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
4. CKE is HIGH for all commands shown except SELF REFRESH and deep power-down.
5. All states and sequences not shown are reserved and/or illegal.
6. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQs column reads a don’t care state to illustrate that the BURST TERMINATE command can occur when there is no data present.
7. Applies only to read and write bursts with auto precharge disabled; this command is undefined and should not be used for READ bursts with auto precharge enabled.
8. This command is a BURST TERMINATE if CKE is HIGH, deep power-down if CKE is LOW.
9. A10 LOW: BA0–BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0–BA1 are “Don’t Care.”
10. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
11. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
12. BA0–BA1 select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA0–BA1 are reserved.) A0–A12 provide the op-code to be written to the selected mode register.

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Load Mode Register

The mode register is loaded via inputs A0–A12, BA0, and BA1. (See "Mode Register" on page 12.) The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in "Burst Type" on page 13.

BURST TERMINATE

The BURST TERMINATE command is used to truncate fixed-length bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in "Operations" on page 22.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAMs. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP has been met after the PRECHARGE command, as shown in "Operations" on page 22.

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The 512Mb SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (^{t}REF). Providing a distributed AUTO REFRESH command every 7.8125µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RFC), once every 64ms.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued every 7.8125µs or less as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Deep Power-Down

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power of the whole memory array of the devices. Array data will not be retained once the device enters deep power-down mode.

This mode is entered by having all banks idle then CS# and WE# held LOW with RAS# and CAS# held HIGH at the rising edge of the clock, while CKE is LOW. This mode is exited by asserting CKE HIGH.

Operations

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 9 on page 23).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 10 on page 23, which covers any case where $2 < {}^{t}RCD\ (MIN)/{}^{t}CK \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 9: Activating a Specific Row in a Specific Bank

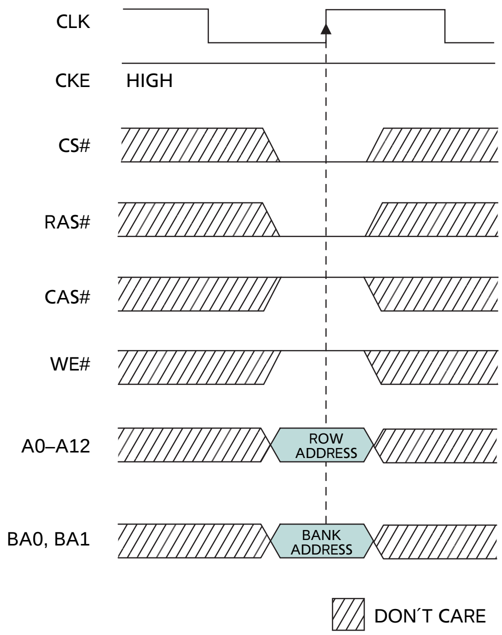
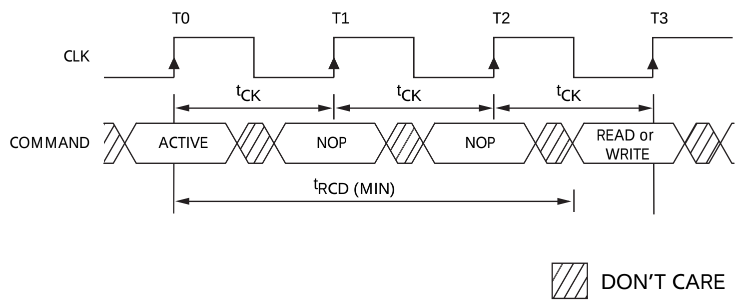


Figure 10: Example: Meeting ^tRCD (MIN) When 2 < ^tRCD (MIN)/$^tCK \leq 3$



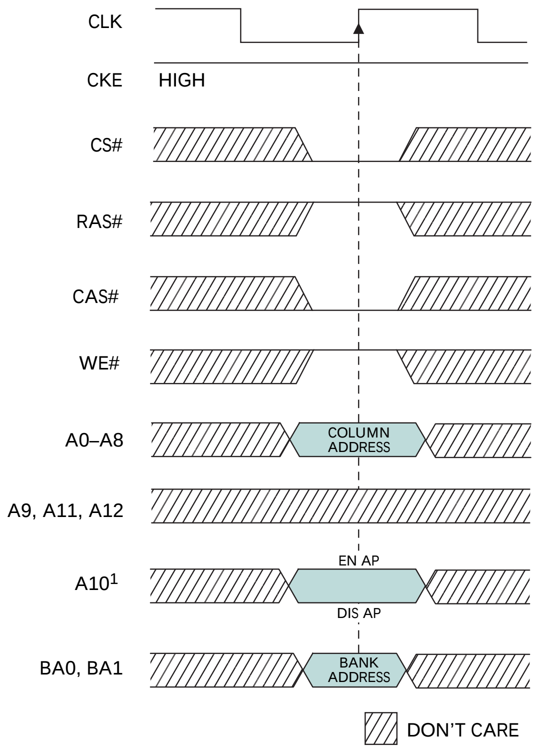
READs

READ bursts are initiated with a READ command, as shown in Figure 11.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CL after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 12 on page 25 shows general timing for each possible CL setting.

Figure 11: READ Command



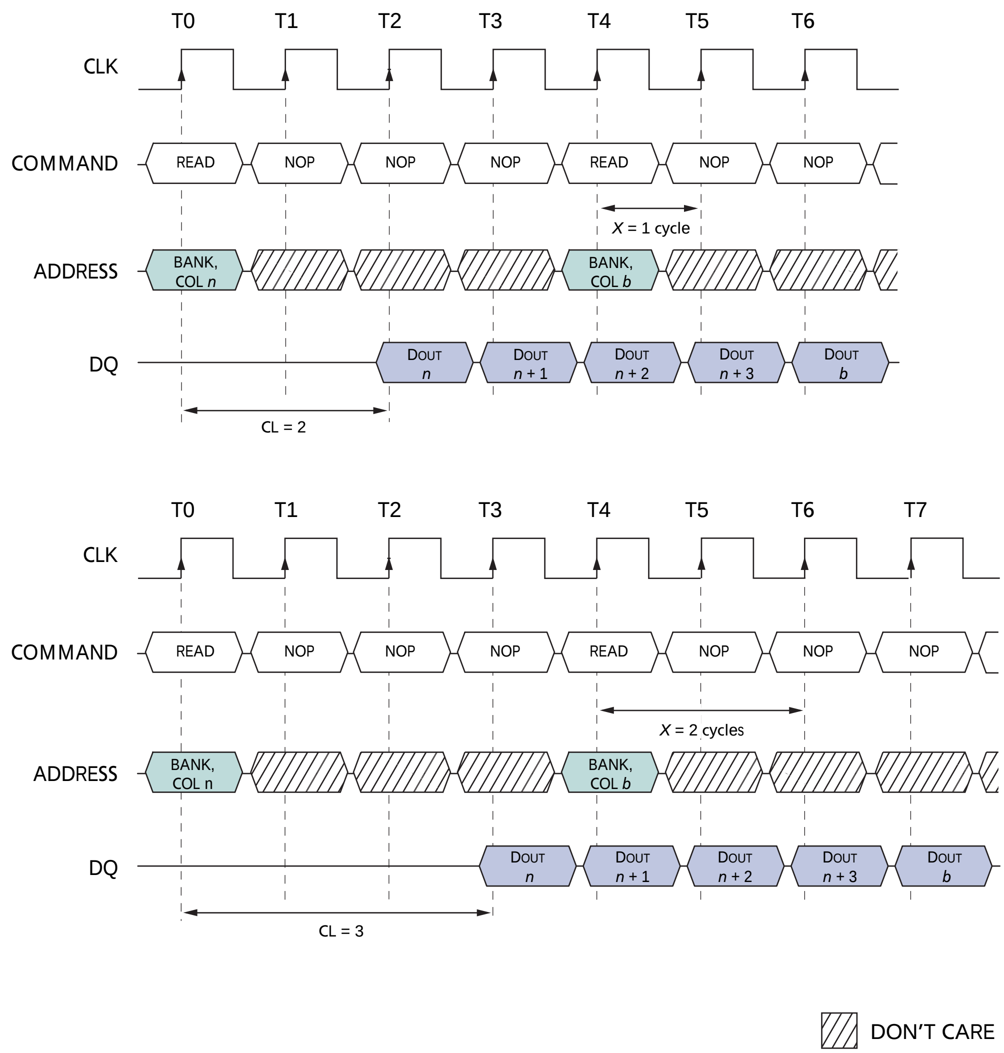
Notes: 1. EN AP = enable auto precharge
DIS AP = disable auto precharge

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued x cycles before the clock edge at which the last desired data element is valid, where x = CL -1.

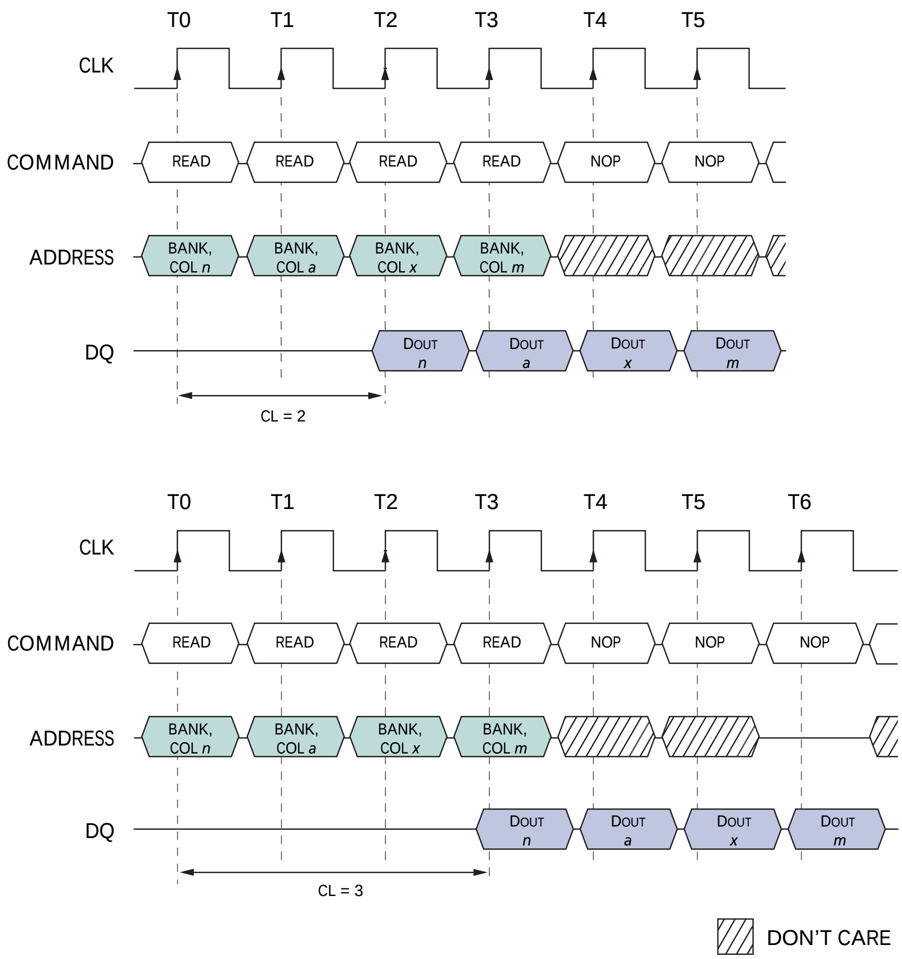
Figure 7 on page 16 shows CLs of two and three; data element $n + 3$ is either the last of a burst of four or the last desired of a longer burst. The 512Mb SDRAM uses a pipelined architecture and therefore does not require the 2n rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 12 on page 25, or each subsequent READ may be performed to a different bank.

Figure 12: Consecutive READ Bursts



Notes: 1. Each READ command may be to any bank. DQM is LOW.

Figure 13: Random READ Accesses



Notes: 1. Each READ command may be to any bank. DQM is LOW.

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

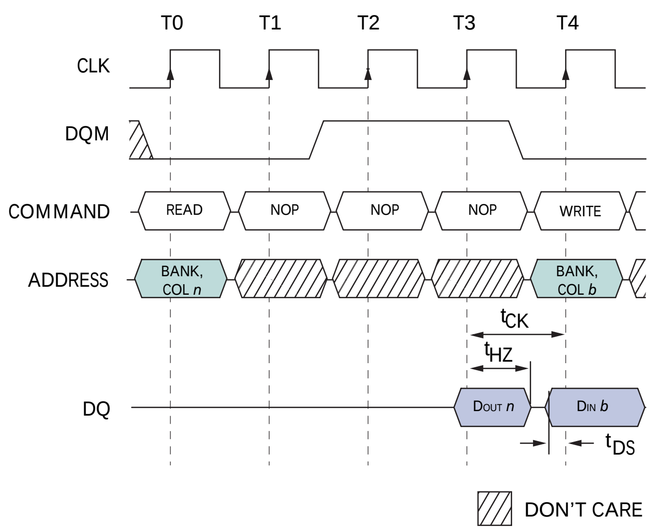
The DQM input is used to avoid I/O contention, as shown in Figure 14 on page 27 and Figure 15 on page 28. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 (in Figure 15 on page 28) then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 13 on page 26 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 15 on page 28 shows the case where the additional NOP is needed.

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 16 on page 28 for each possible CL; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

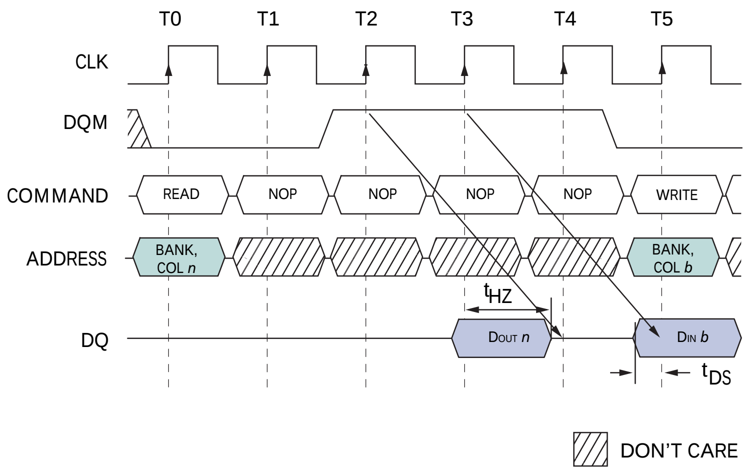
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts.

Figure 14: READ-to-WRITE



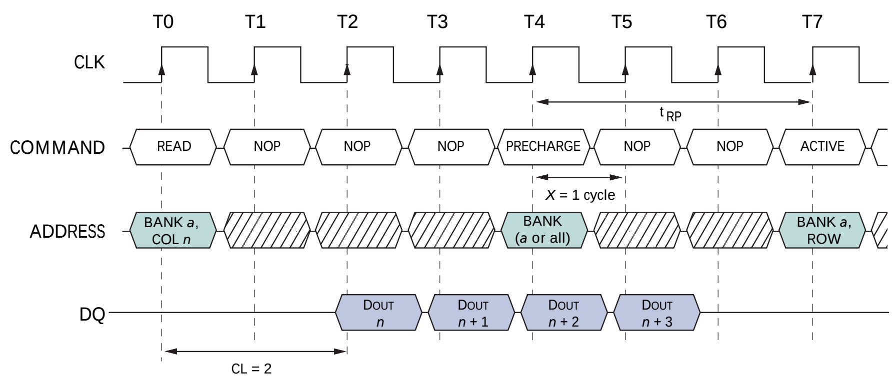
Notes: 1. CL = 3. The READ command may be to any bank, and the WRITE command may be to any bank. If a burst of one is used, then DQM is not required.

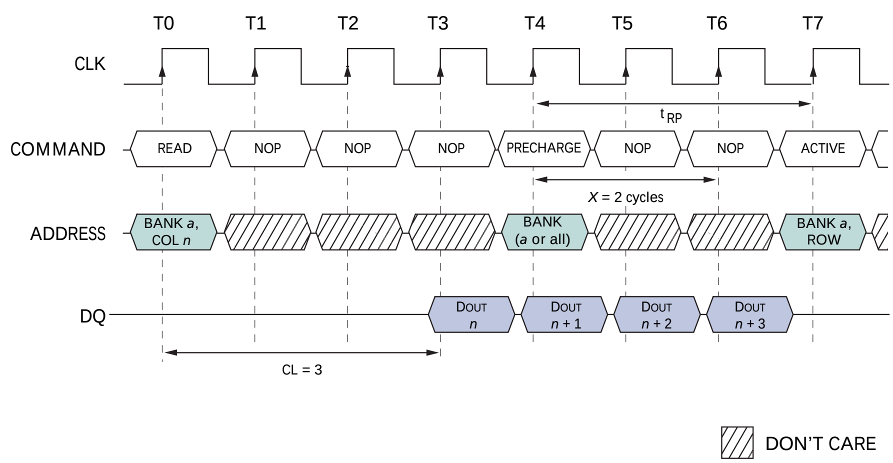
Figure 15: READ-to-WRITE with Extra Clock Cycle



Notes: 1. CL = 3. The READ command may be to any bank, and the WRITE command may be to any bank.

Figure 16: READ-to-PRECHARGE

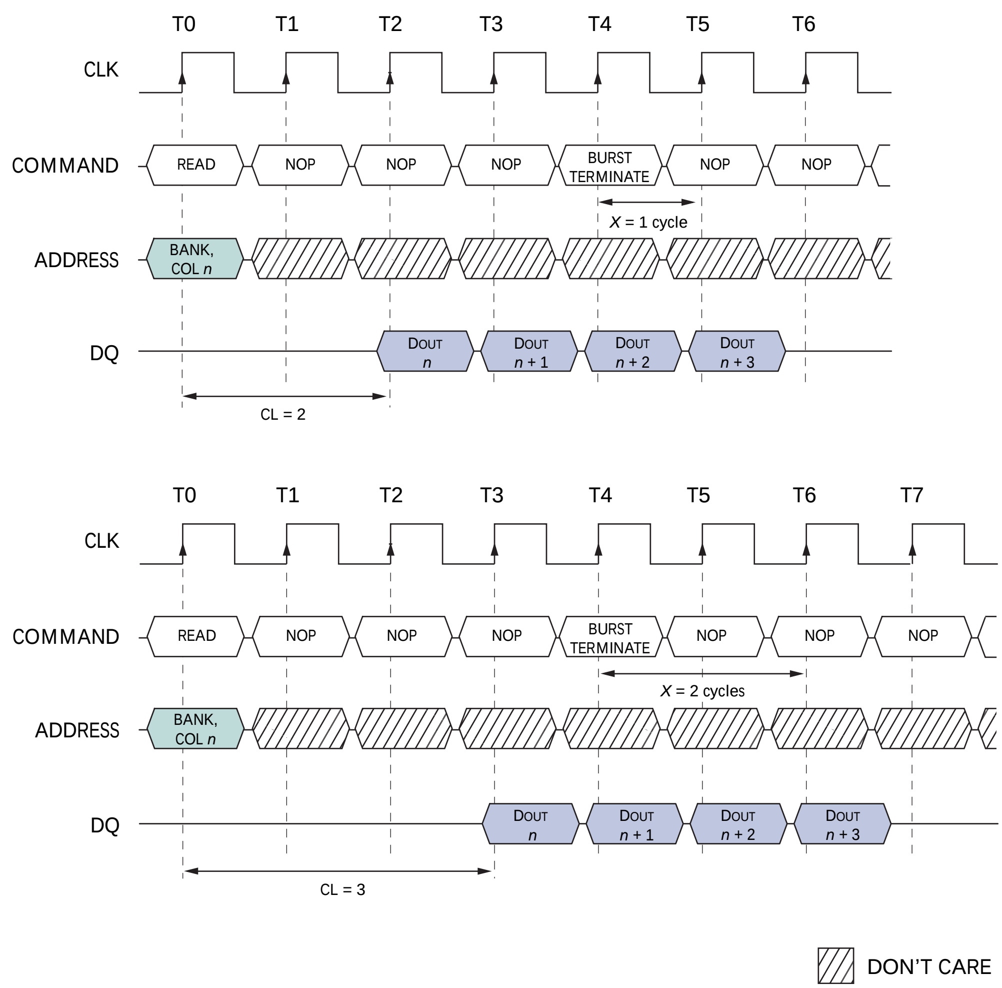




Notes: 1. DQM is LOW.

Fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. This is shown in Figure 17 on page 29 for each possible CL; data element n + 3 is the last desired data element of a longer burst.

Figure 17: Terminating a READ Burst



Notes: 1. DQM is LOW.

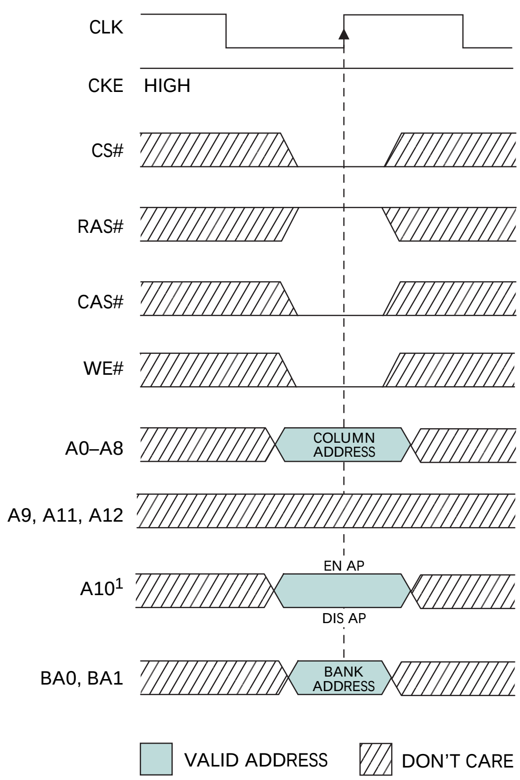
WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 18.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see Figure 19 on page 31).

Figure 18: WRITE Command

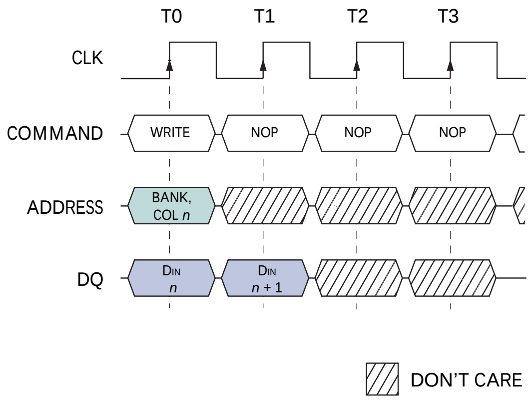


Notes: 1. EN AP = enable auto precharge
DIS AP = disable auto precharge

Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 20 on page 31. Data $n + 1$ is either the last of a burst of two or the last desired of a longer burst. The 512Mb SDRAM uses a pipelined architecture and therefore does not require the $2n$ rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous

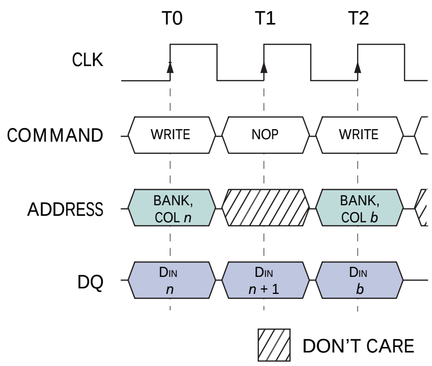
WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 21 on page 32, or each subsequent WRITE may be performed to a different bank.

Figure 19: WRITE Burst



Notes: 1. BL = 2. DQM is LOW.

Figure 20: WRITE-to-WRITE



Notes: 1. DQM is LOW. Each WRITE command may be to any bank.

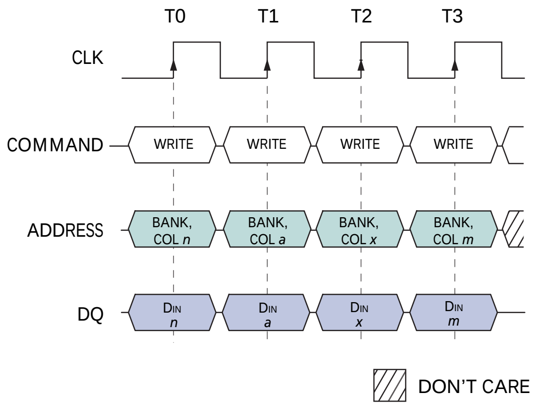
Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is registered, the data inputs will be ignored, and WRITEs will not be executed. An example is shown in Figure 22 on page 32. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock plus time, regardless of frequency.

In addition, when truncating a WRITE burst at high clock frequencies (^{t}CK < 15ns), the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 23 on page 33. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

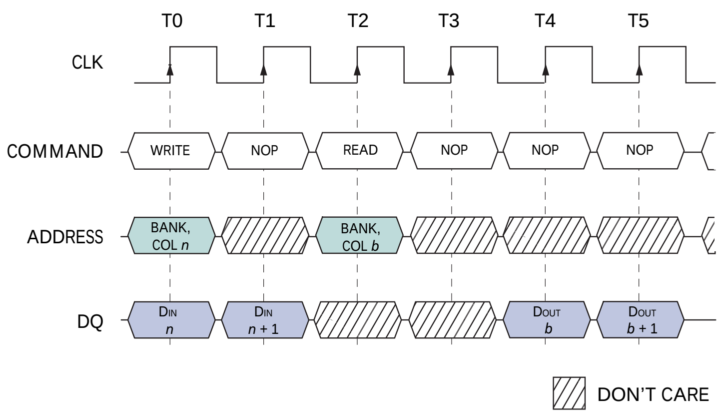
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts.

Figure 21: Random WRITE Cycles



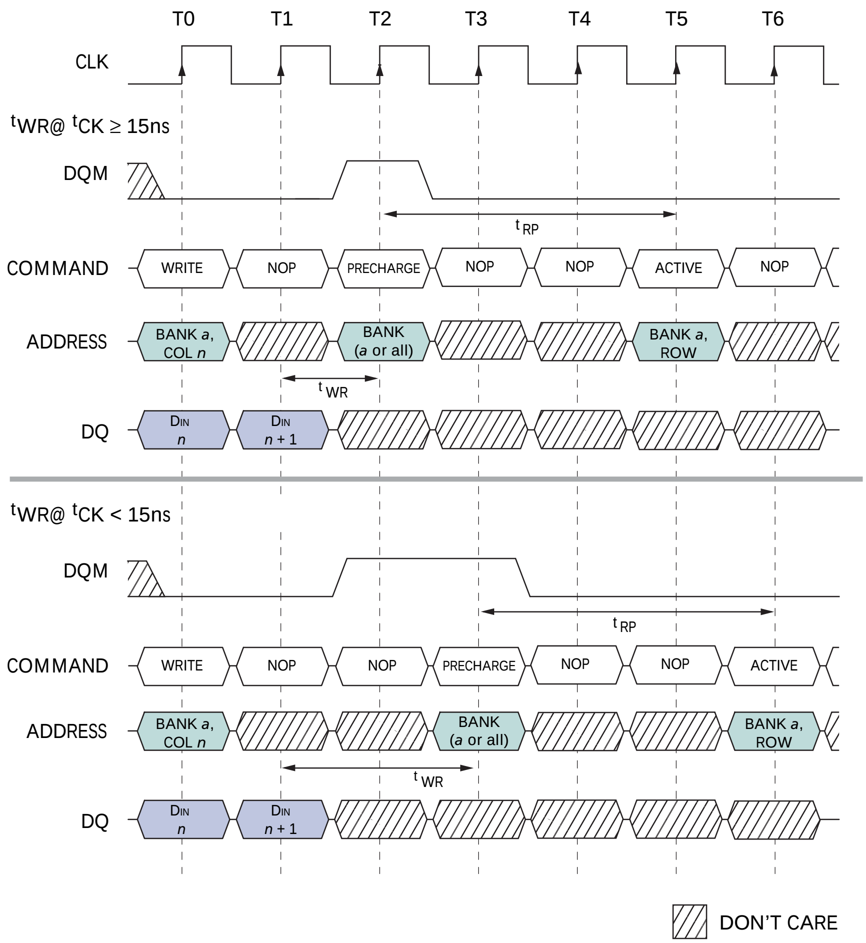
Notes: 1. Each WRITE command may be to any bank. DQM is LOW.

Figure 22: WRITE-to-READ



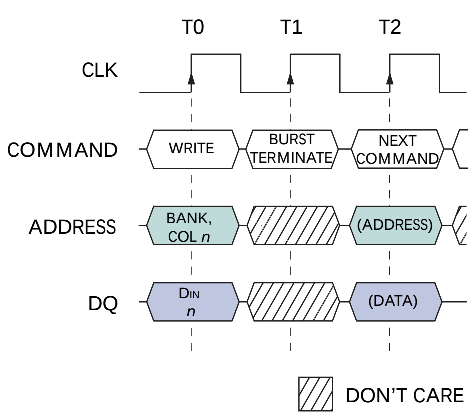
Notes: 1. The WRITE command may be to any bank, and the READ command may be to any bank. DQM is LOW. CL = 2 for illustration.

Figure 23: WRITE-to-PRECHARGE



Notes: 1. DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

Figure 24: Terminating a WRITE Burst

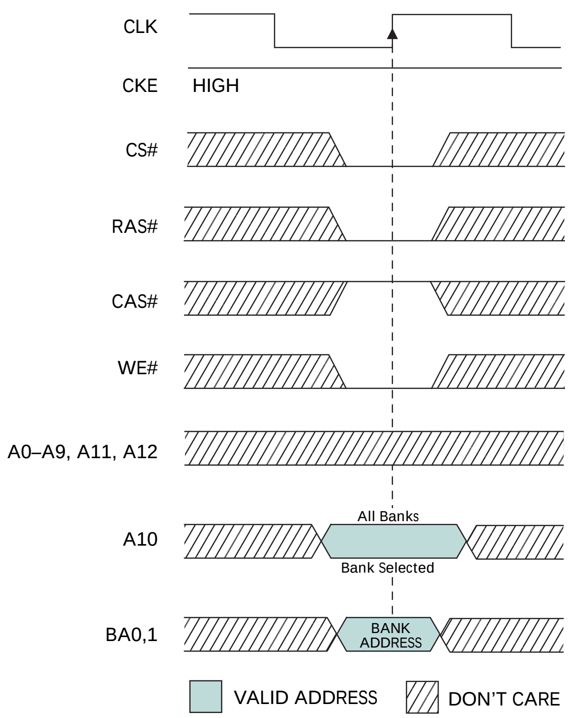


Fixed-length WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 24 on page 33, where data *n* is the last desired data element of a longer burst.

PRECHARGE

The PRECHARGE command (see Figure 25 on page 34) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 25: PRECHARGE Command

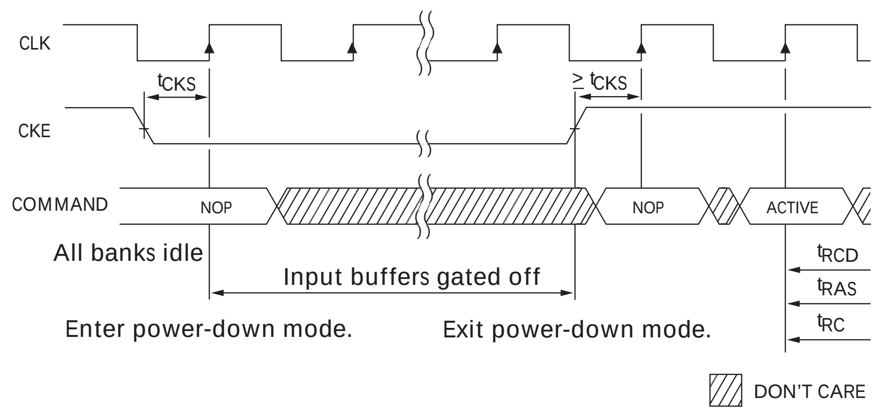


Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no REFRESH operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting ${}^tCKS$). See Figure 28 on page 36.

Figure 26: Power-Down



Deep Power-Down

Deep power-down mode is a maximum power savings feature achieved by shutting off the power to the entire memory array of the device. Data on the memory array will not be retained once deep power-down mode is executed. Deep power-down mode is entered by having all banks idle then CS# and WE# held LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during deep power-down.

Figure 27: Deep Power-Down Command

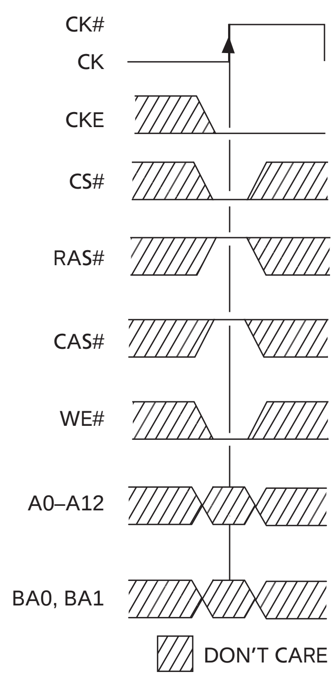
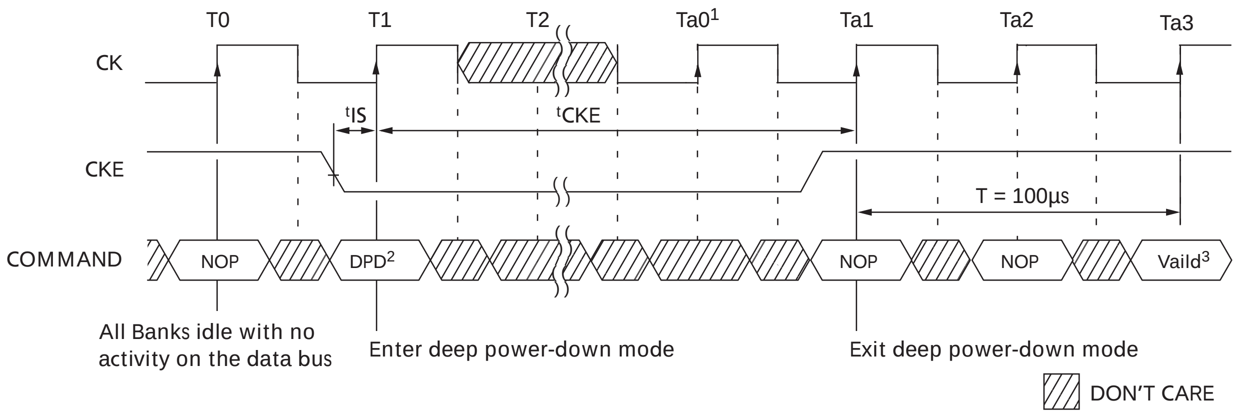


Figure 28: Deep Power-Down



Notes:
1. Clock must be stable prior to CKE going HIGH.
2. DPD = Deep power-down mode command; PRE ALL = Precharge all banks.
3. Exit of deep power-down mode must be followed by the sequence described in the Deep Power-Down" section on page 35.

In order to exit deep power-down mode, CKE must be asserted HIGH. After exiting, the following sequence is needed in order to enter a new command:

1. Maintain NOP input conditions for a minimum of 100µs.
2. Issue PRECHARGE commands for all banks.
3. Issue two or more AUTO REFRESH commands.

The values of the mode register and extended mode register will be retained upon exiting deep power-down.

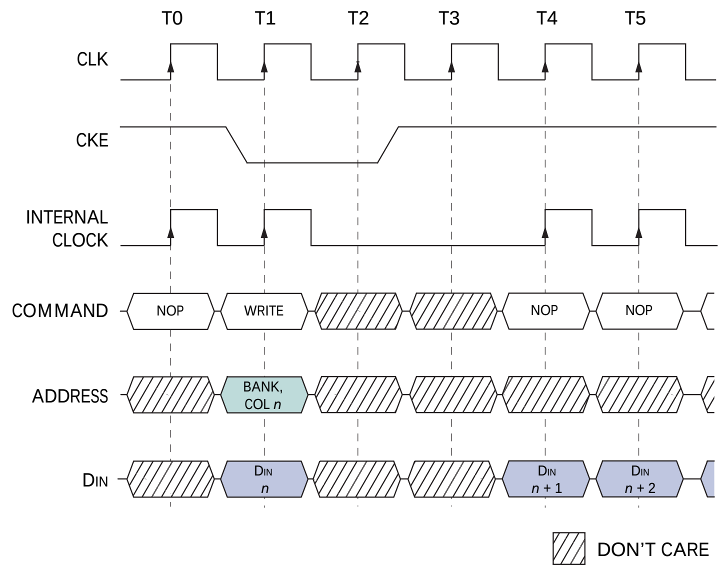
Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls at the time of a suspended internal clock edge is ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended (see examples in Figure 29 on page 37 and Figure 30 on page 37).

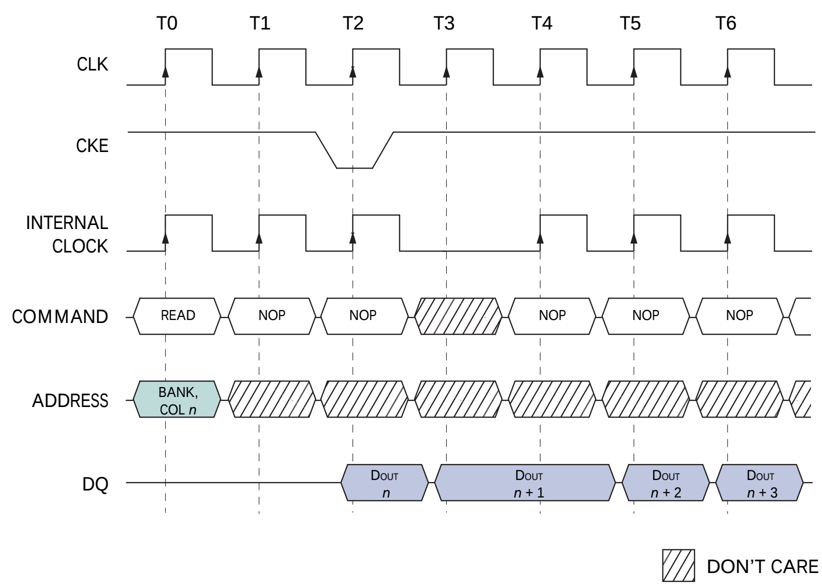
Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

Figure 29: Clock Suspend During WRITE Burst



Notes: 1. For this example, BL = 4 or greater, and DQM is LOW.

Figure 30: Clock Suspend During READ Burst



Notes: 1. For this example, CL = 2, BL = 4 or greater, and DQM is LOW.

Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed BL. READ commands access columns according to the programmed BL and sequence, just as in the normal mode of operation.

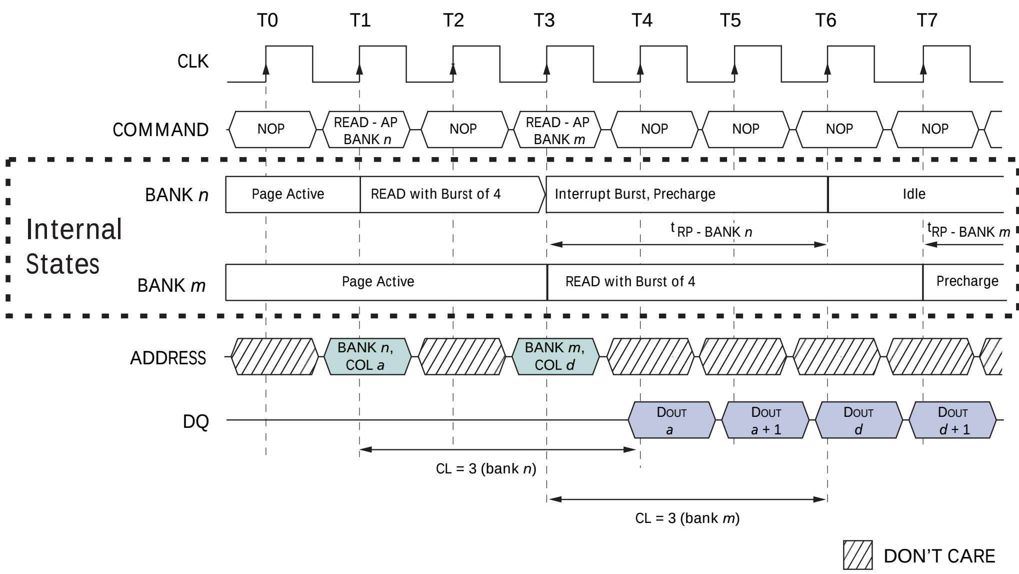
Concurrent Auto Precharge

An access command (READ or WRITE) to a second bank while an access command with auto precharge enabled on a first bank is executing is not allowed by SDRAMs, unless the SDRAM supports concurrent auto precharge. Micron SDRAMs support concurrent auto precharge. Four cases where concurrent auto precharge occurs are defined below.

READ with Auto Precharge

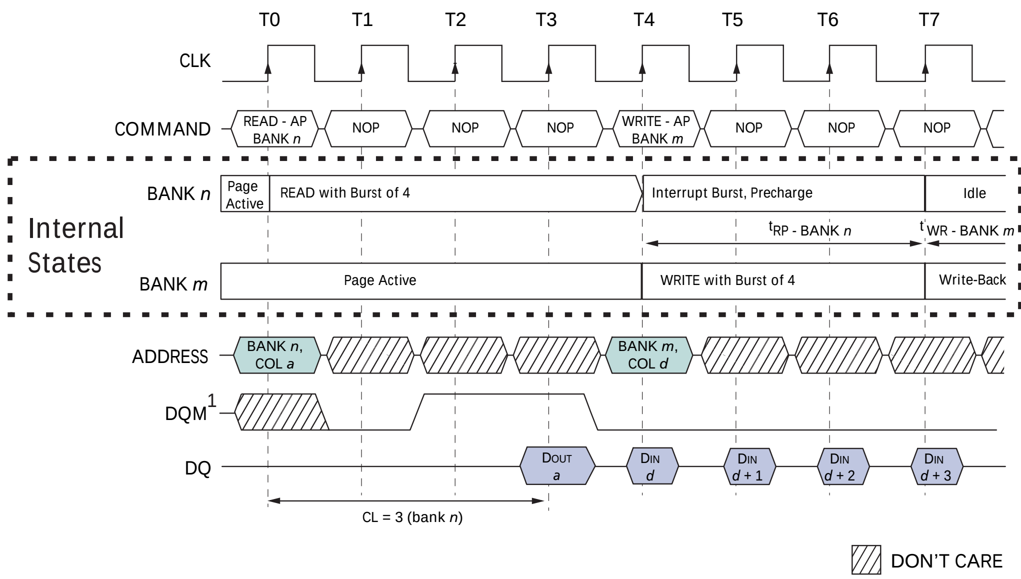
1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ on bank *n*, CL later. The precharge to bank *n* will begin when the READ to bank *m* is registered (Figure 31).
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank *n* will begin when the WRITE to bank *m* is registered (Figure 32 on page 39).

Figure 31: READ With Auto Precharge Interrupted by a READ



Notes: 1. DQM is LOW.

Figure 32: READ With Auto Precharge Interrupted by a WRITE

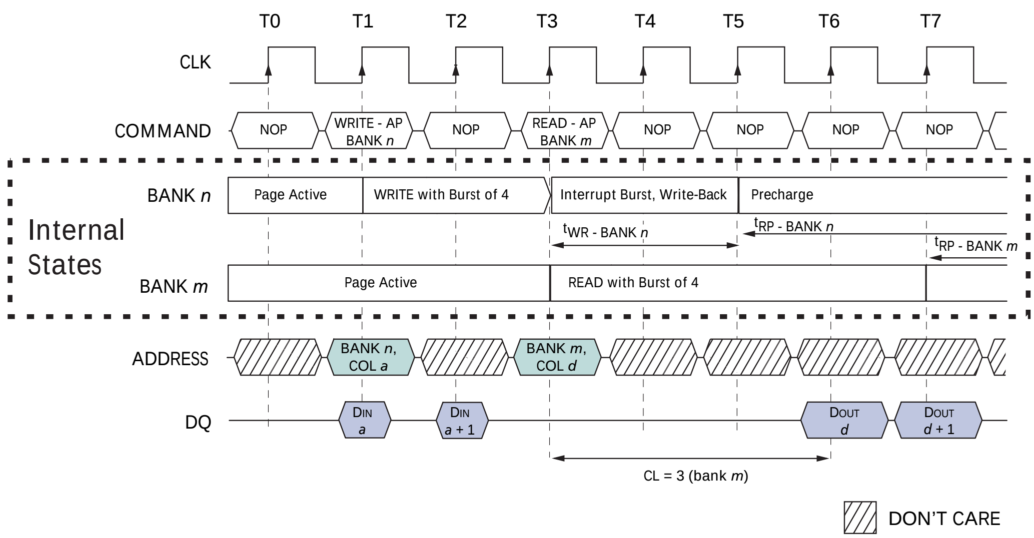


Notes: 1. DQM is HIGH at T2 to prevent DOUT *a* + 1 from contending with DIN *d* at T4.

WRITE with Auto Precharge

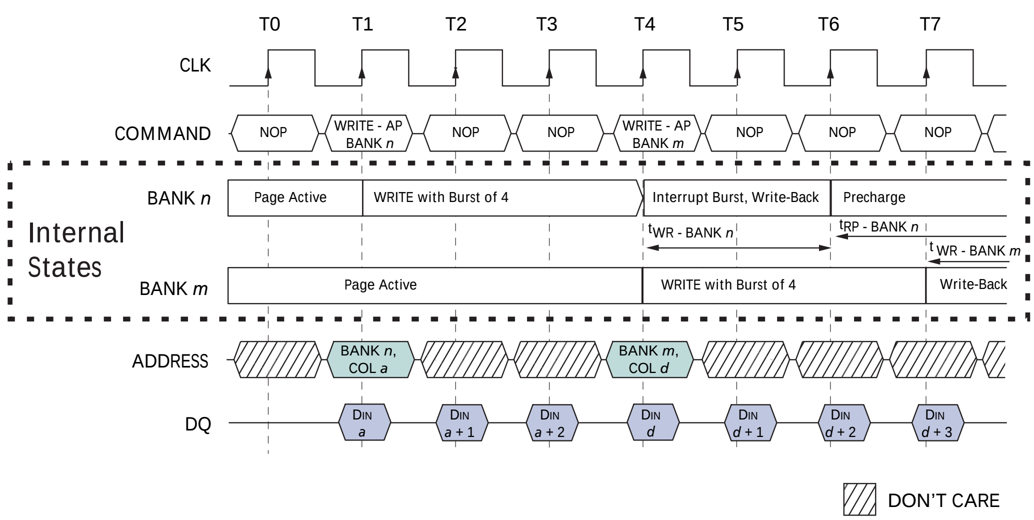
1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CL later. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 33).
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (Figure 34).

Figure 33: WRITE With Auto Precharge Interrupted by a READ



Notes: 1. DQM is LOW.

Figure 34: WRITE With Auto Precharge Interrupted by a WRITE



Notes: 1. DQM is LOW.

Truth Tables

Table 6: Truth Table – CKE

Notes: 1–4

CKE_{n-1}	CKE_n	Current State	$Command_n$	$Action_n$	Notes
L	L	Power-Down	X	Maintain power-down	
		Self refresh	X	Maintain self refresh	
		Clock suspend	X	Maintain clock suspend	
		Deep power-down	X	Maintain deep power-down	5
L	H	Power-Down	COMMAND INHIBIT or NOP	Exit power-down	6
		Deep power-down	X	Exit deep power-down	5
		Self refresh	COMMAND INHIBIT or NOP	Exit self refresh	7
		Clock suspend	X	Exit clock suspend	8
H	L	All banks idle	COMMAND INHIBIT or NOP	Power-Down entry	
		All banks idle	BURST TERMINATE	Deep power-down entry	5
		All banks idle	AUTO REFRESH	Self refresh entry	
		Reading or writing	VALID	Clock suspend entry	
H	H		Table 8 on page 44		

Notes:
1. CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Deep power-down is power savings feature of this Mobile SDRAM device. This command is BURST TERMINATE when CKE is HIGH and deep power-down when CKE is LOW.
6. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that ^tCKS is met).
7. Exiting self refresh at clock edge *n* will put the device in the all banks idle state once ^tXSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^tXSR period. A minimum of two NOP commands must be provided during the ^tXSR period.
8. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n* + 1.

Table 7: Truth Table – Current State Bank *n*, Command to Bank *n*
Notes: 1–6; notes appear below table

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	8
Row active	L	H	L	H	READ (Select column and start READ burst)	9
	L	H	L	L	WRITE (Select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	10
Read (auto precharge disabled)	L	H	L	H	READ (Select column and start new READ burst)	9
	L	H	L	L	WRITE (Select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	10
	L	H	H	L	BURST TERMINATE	11
Write (auto precharge disabled)	L	H	L	H	READ (Select column and start READ burst)	9
	L	H	L	L	WRITE (Select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	10
	L	H	H	L	BURST TERMINATE	11

Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 6 on page 41) and after ^tXSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 7, and according to Table 8 on page 44.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^tRP is met. Once ^tRP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. Once ^tRCD is met, the bank will be in the row active state.

   Read w/auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

   Write w/auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

Refreshing:	Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. Once ^{t}RFC is met, the SDRAM will be in the all banks idle state.
Accessing mode register:	Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the Mobile SDRAM will be in the all banks idle state.
Precharging all:	Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. Does not affect the state of the bank and acts as a NOP to that bank.
9. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
10. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
11. This command is BURST TERMINATE when CKE is HIGH.

Table 8: Truth Table – Current State Bank *n*, Command to Bank *m*
Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 8
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	10
Write (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 11
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 12
	L	L	H	L	PRECHARGE	10
Read (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 13, 14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 13, 15
	L	L	H	L	PRECHARGE	10
Write (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 13, 16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 13, 17
	L	L	H	L	PRECHARGE	10

Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (Table 6 on page 41) and after ^tXSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Read w/auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

   Write w/auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.
4. AUTO REFRESH, SELF REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.

5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later (Figure 11 on page 24).
9. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used one clock prior to the WRITE command to prevent bus contention.
10. Burst in bank *n* continues as initiated.
11. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
12. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank will interrupt the WRITE on bank *n* when registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. Concurrent auto precharge: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m* burst.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered.
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered.
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE bank *n* will be data-in registered one clock prior to the READ to bank *m*.
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock to the WRITE to bank *m*.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in Table 9 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 9: Absolute Maximum Ratings

Voltage/Temperature	Min	Max	Units
Voltage on $V_{DD}/V_{DD}Q$ supply relative to V_{SS}	–0.3	+2.7	V
Voltage on inputs, NC or I/O balls relative to V_{SS}	–0.3	+2.7	
Storage temperature plastic	–55	+150	°C

Table 10: DC Electrical Characteristics and Operating Conditions
Notes: 1, 5, 6; notes appear on pages 51–52

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.95	V	
I/O supply voltage	$V_{DD}Q$	1.7	1.95	V	
Input high voltage: Logic 1; All inputs	V_{IH}	0.8 × $V_{DD}Q$	$V_{DD}Q$ + 0.3	V	22
Input low voltage: Logic 0; All inputs	V_{IL}	–0.3	+0.3	V	22
Output high voltage:	V_{OH}	0.9 × $V_{DD}Q$	–	V	28
Output low voltage:	V_{OL}	–	0.2	V	28
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)	I_I	–1.0	1.0	µA	
Operating temperature Commercial Industrial	 T_A T_A	 0 –40	 +70 +85	°C	

Table 11: Electrical Characteristics and Recommended AC Operating Conditions
Notes: 5, 6, 8, 9, 11; notes appear on pages 51–52

AC Characteristics			-75		-8			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Access time from CLK (pos. edge)	CL = 3	^{t}AC (3)		6		7	ns	
	CL = 2	^{t}AC (2)		9		9	ns	
Address hold time		^{t}AH	1		1		ns	
Address setup time		^{t}AS	1.5		2.5		ns	
CLK high-level width		^{t}CH	3		3		ns	
CLK low-level width		^{t}CL	3		3		ns	
Clock cycle time	CL = 3	^{t}CK (3)	7.5		8		ns	23
	CL = 2	^{t}CK (2)	9.6		10		ns	23
CKE hold time		^{t}CKH	1		1		ns	
CKE setup time		^{t}CKS	2.5		2.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	1.5		2.5		ns	
Data-in hold time		^{t}DH	1		1		ns	
Data-in setup time		^{t}DS	1.5		2.5		ns	
Data-out High-Z time	CL = 3	^{t}HZ (3)		6		7	ns	10
	CL = 2	^{t}HZ (2)		9		9	ns	10
Data-out Low-Z time		^{t}LZ	1		1		ns	
Data-out hold time (load)		^{t}OH	2.5		2.5		ns	
ACTIVE-to-PRECHARGE command		^{t}RAS	44	120,000	48	120,000	ns	
ACTIVE-to-ACTIVE command period		^{t}RC	67.5		72		ns	
ACTIVE-to-READ or WRITE delay		^{t}RCD	19		20		ns	
Refresh period (8,192 rows)		^{t}REF		64		64	ms	
AUTO REFRESH period		^{t}RFC	80		80		ns	
PRECHARGE command period		^{t}RP	19		19		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	2		2		^{t}CK	
Transition time		^{t}T	0.3	1.2	0.5	1.2	ns	7
WRITE recovery time		^{t}WR	15		15		ns	31
Exit SELF REFRESH-to-ACTIVE command		^{t}XSR	80		80		ns	20

Table 12: AC Functional Characteristics
Notes: 5, 6, 8, 9,11; notes appear on pages 51–52

Parameter		Symbol	-75	-8	Units	Notes
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	^{t}CK	17
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	^{t}CK	14
CKE to clock enable or power-down exit mode		^{t}PED	1	1	^{t}CK	14
DQM to input data delay		^{t}DQD	0	0	^{t}CK	17
DQM to data mask during WRITEs		^{t}DQM	0	0	^{t}CK	17
DQM to data High-Z during READs		^{t}DQZ	2	2	^{t}CK	17
WRITE command to input data delay		^{t}DWD	0	0	^{t}CK	17
Data-in to ACTIVE command		^{t}DAL	5	5	^{t}CK	15, 21
Data-in to PRECHARGE command		^{t}DPL	2	2	^{t}CK	16, 21
Last data-in to burst STOP command		^{t}BDL	1	1	^{t}CK	17
Last data-in to new READ/WRITE command		^{t}CDL	1	1	^{t}CK	17
Last data-in to PRECHARGE command		^{t}RDL	2	2	^{t}CK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	^{t}CK	25
Data-out High-Z from PRECHARGE command	CL = 3	^{t}ROH(3)	3	3	^{t}CK	17
	CL = 2	^{t}ROH(2)	2	2	^{t}CK	17

Table 13: I_{DD} Specifications and Conditions (x16)

Notes: 1, 5, 6, 11, 13; notes appear on pages 51–52; V_{DD} = 1.7V to 1.95V, $V_{DD}Q$ = 1.7V to 1.95V

Parameter/Condition		Symbol	Max -75	Max -8	Units	Notes
Operating current: Active mode; Burst = 1; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}	95	90	mA	18, 19
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2P} Standard	500	500	µA	29
		I_{DD2P} Low Power	300	300		
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		I_{DD2N}	20	20	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		I_{DD3P}	20	20	mA	12, 19
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3N}	30	30	mA	12, 19
Operating current: Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle		I_{DD4}	90	85	mA	18, 19
Auto refresh current CKE = HIGH; CS# = HIGH	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}	85	80	mA	12, 18, 19, 26
	^{t}RFC = 7.8125µs	I_{DD6}	5	5	mA	
Deep power-down		I_{ZZ}	10	10	µA	29, 30

Table 14: I_{DD} Specifications and Conditions (x32)

Notes: 1, 5, 6, 11, 13; notes appear on pages 51–52; V_{DD} = 1.7V to 1.95V, $V_{DD}Q$ = 1.7V to 1.95V

Parameter/Condition		Symbol	Max -75	Max -8	Units	Notes
Operating current: Active mode; Burst = 1; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}	115	110	mA	18, 19
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2P} Standard	500	500	µA	29
		I_{DD2P} Low Power	300	300		
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		I_{DD2N}	20	20	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		I_{DD3P}	20	20	mA	12, 19
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3N}	30	30	mA	12, 19
Operating current: Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle		I_{DD4}	120	115	mA	18, 19
Auto refresh current CKE = HIGH; CS# = HIGH	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}	85	80	mA	12, 18, 19, 26
	^{t}RFC = 7.8125µs	I_{DD6}	5	5	mA	
Deep power-down		I_{ZZ}	10	10	µA	29, 30

Table 15: IDD7 Specifications and Conditions (x16 and x32)
Notes:1–6, 8, 11, 13, 15, 27; notes appear on pages 51–52; VDD/VDDQ = 1.70–1.95V

Parameter/Condition		Symbol	Low IDD7 Option "L"	Standard IDD7 Option	Units	Notes
Self refresh CKE = LOW; ${}^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are stable; Data bus inputs are stable.	Full array, 85°C	IDD7a	300	500	µA	17, 29
	Full array, 70°C	IDD7b	230	430	µA	
	Full array, 45°C	IDD7c	180	380	µA	
	Full array, 15°C	IDD7d	160	360	µA	
	Half array, 85°C	IDD7a	250	440	µA	
	Half array, 70°C	IDD7b	200	380	µA	
	Half array, 45°C	IDD7c	170	350	µA	
	Half array, 15°C	IDD7d	150	330	µA	
	1/4 array, 85°C	IDD7a	210	410	µA	
	1/4 array, 70°C	IDD7b	175	365	µA	
	1/4 array, 45°C	IDD7c	155	335	µA	
	1/4 array, 15°C	IDD7d	140	305	µA	
	1/8 array, 85°C	IDD7a	180	390	µA	
	1/8 array, 70°C	IDD7b	155	350	µA	
	1/8 array, 45°C	IDD7c	145	315	µA	
	1/8 array, 15°C	IDD7d	135	300	µA	
	1/16 array, 85°C	IDD7a	170	380	µA	
	1/16 array, 70°C	IDD7b	145	340	µA	
	1/16 array, 45°C	IDD7c	135	320	µA	
	1/16 array, 15°C	IDD7d	130	290	µA	

Figure 35: Typical Self Refresh Current vs. Temperature

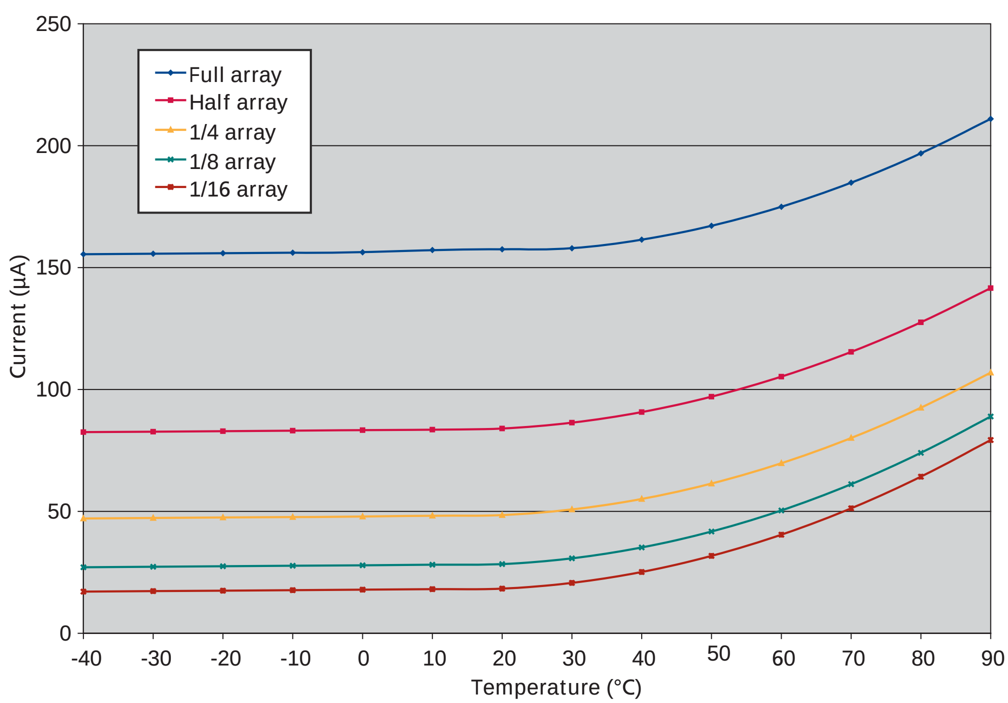


Table 16: Capacitance (x16)
Note: 2; notes appear on pages 51–52

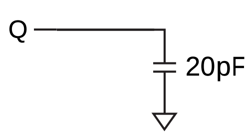
Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	CI1	2.0	5.0	pF
Input capacitance: All other input-only balls	CI2	2.0	5.0	pF
Input/Output capacitance: DQs	CIO	2.5	6.0	pF

Table 17: Capacitance (x32)
Note: 2; notes appear on pages 51–52

Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	CI1	2.0	5.0	pF
Input capacitance: All other input-only balls	CI2	2.0	5.0	pF
Input/Output capacitance: DQs	CIO	2.5	6.0	pF

Notes

1. All voltages referenced to VSS.
2. This parameter is sampled. VDD, VDDQ = +1.8V; T_A = 25°C; ball under test biased at 0.9V, 1.25V, and 1.4V, respectively; f = 1 MHz.
3. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (–40°C ≤ T_A ≤ +85°C for T_A on IT parts) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VDD and VDDQ must be powered up simultaneously. VSS and VSSQ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
9. Outputs measured for 1.8V at 0.9V with equivalent load:

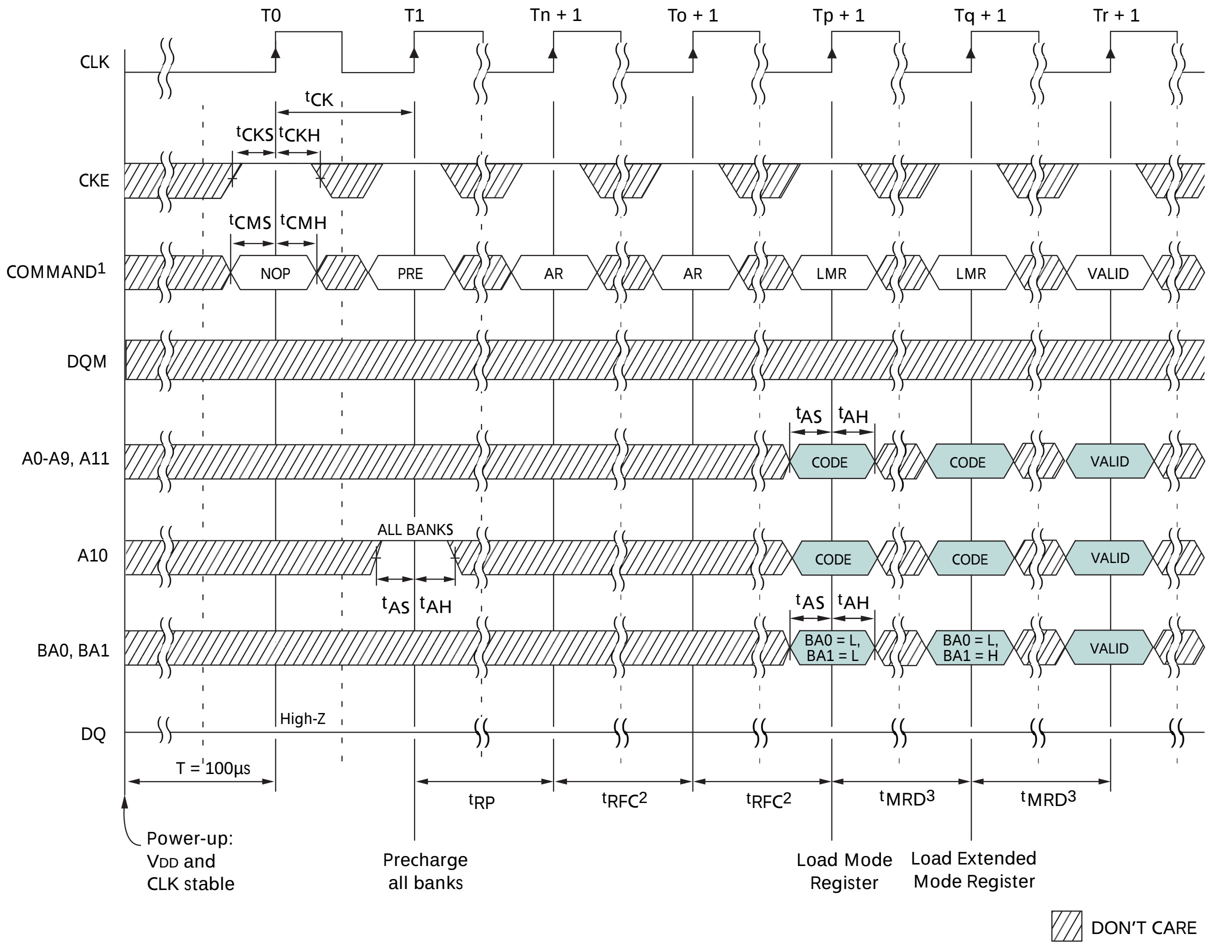
   

   Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.
10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and IDD tests have VIL and VIH, with timing referenced to VIH/2 = crossover point. If the input transition time is longer than ^{t}T (MAX), then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the VIH/2 crossover point.

12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^tCKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^tWR plus ^tRP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^tWR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^tCK = 7.5ns for -75, and ^tCK = 8ns for -8, CL = 3.
22. V_{IH} overshoot: V_{IH} (MAX) = V_{DDQ} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = –2V for a pulse width ≤ 3ns.
23. The only time that the clock frequency is allowed to change is during clock stop, power down, or self-refresh modes.
24. Auto precharge mode only. The precharge timing budget (^tRP) begins at 7ns for -8 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Parameter guaranteed by design.
26. CKE is HIGH during refresh command period ^tRFC (MIN), else CKE is LOW. The $I_{DD}7$ limit is actually a nominal value and does not result in a fail value.
27. Values for $I_{DD}7$ for 85°C are 100 percent tested. Values for 70°C, 45°C, and 15°C are sampled only.
28. I_{OUT} = 4mA for full-drive strength. Other drive strengths require appropriate scale.
29. Current is taken 500ms after entering into this operating mode to allow tester measuring unit settling time.
30. Deep power-down current is a nominal value at 25°C. This parameter is not tested.
31. There must be one ^tCK during the ^tWR time for WRITE auto precharge.

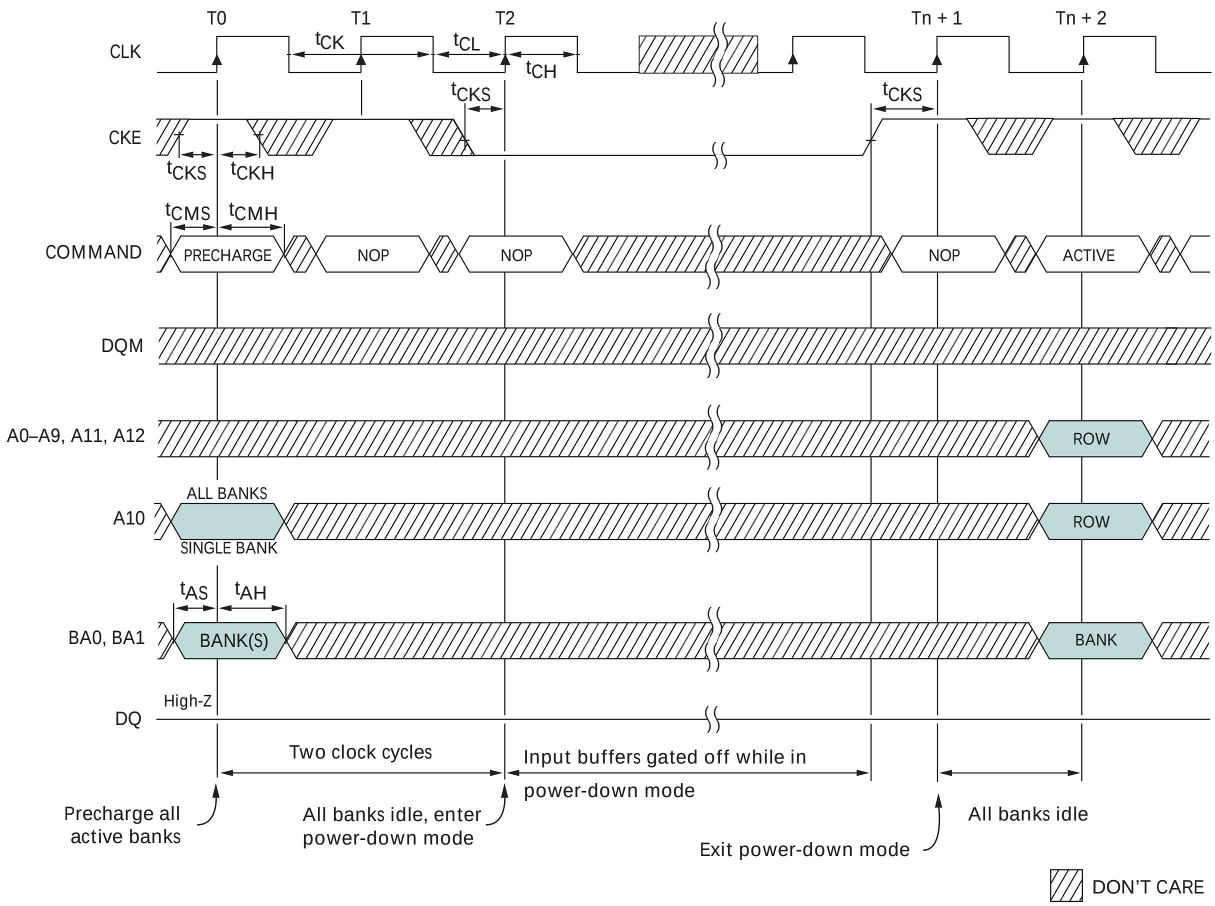
Timing Diagrams

Figure 36: Initialize and Load Mode Register



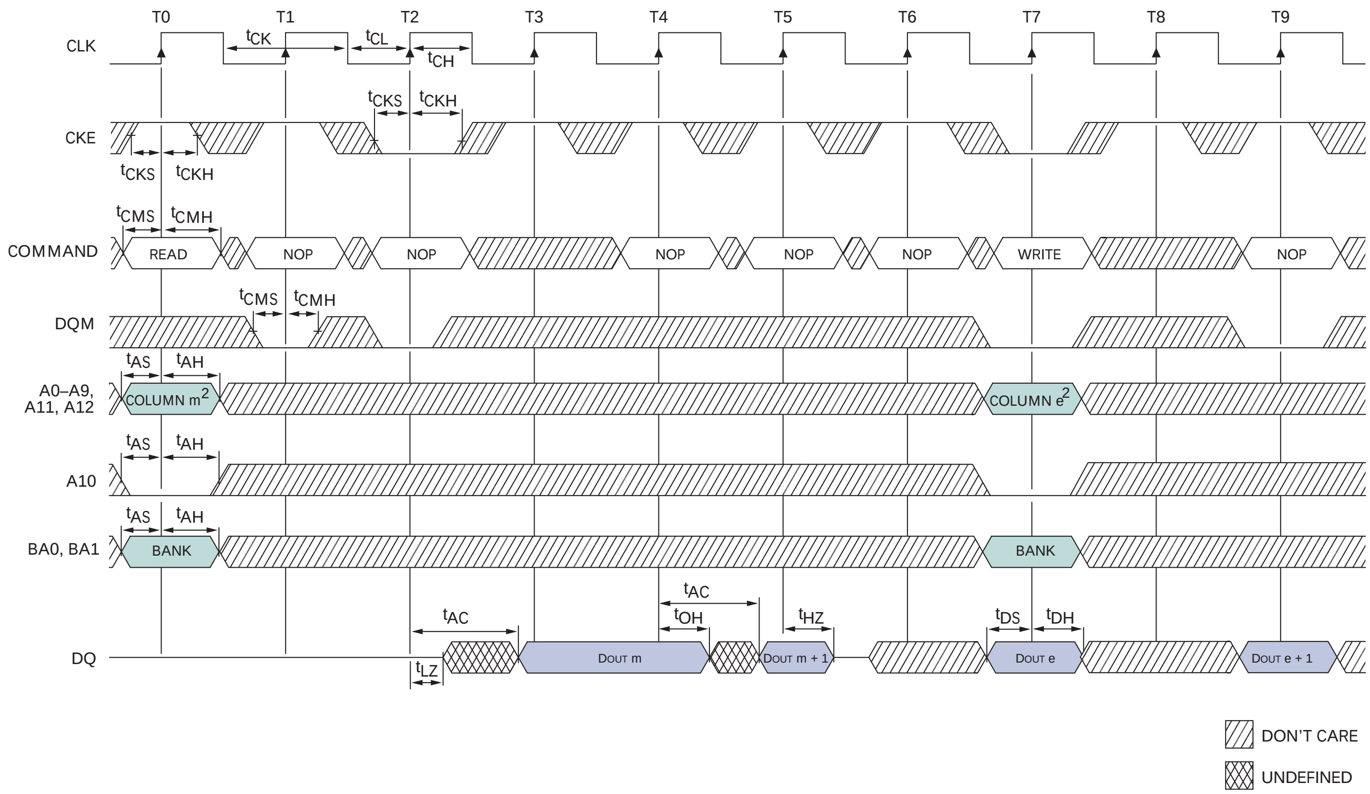
Notes:
1. PRE = PRECHARGE command, AR = AUTO REFRESH command, LMR = LOAD MODE REGISTER command.
2. Only NOPs or COMMAND INHIBITs may be issued during ^{t}RFC time.
3. At least one NOP or COMMAND INHIBIT is required during ^{t}MRD time.

Figure 37: Power-Down Mode



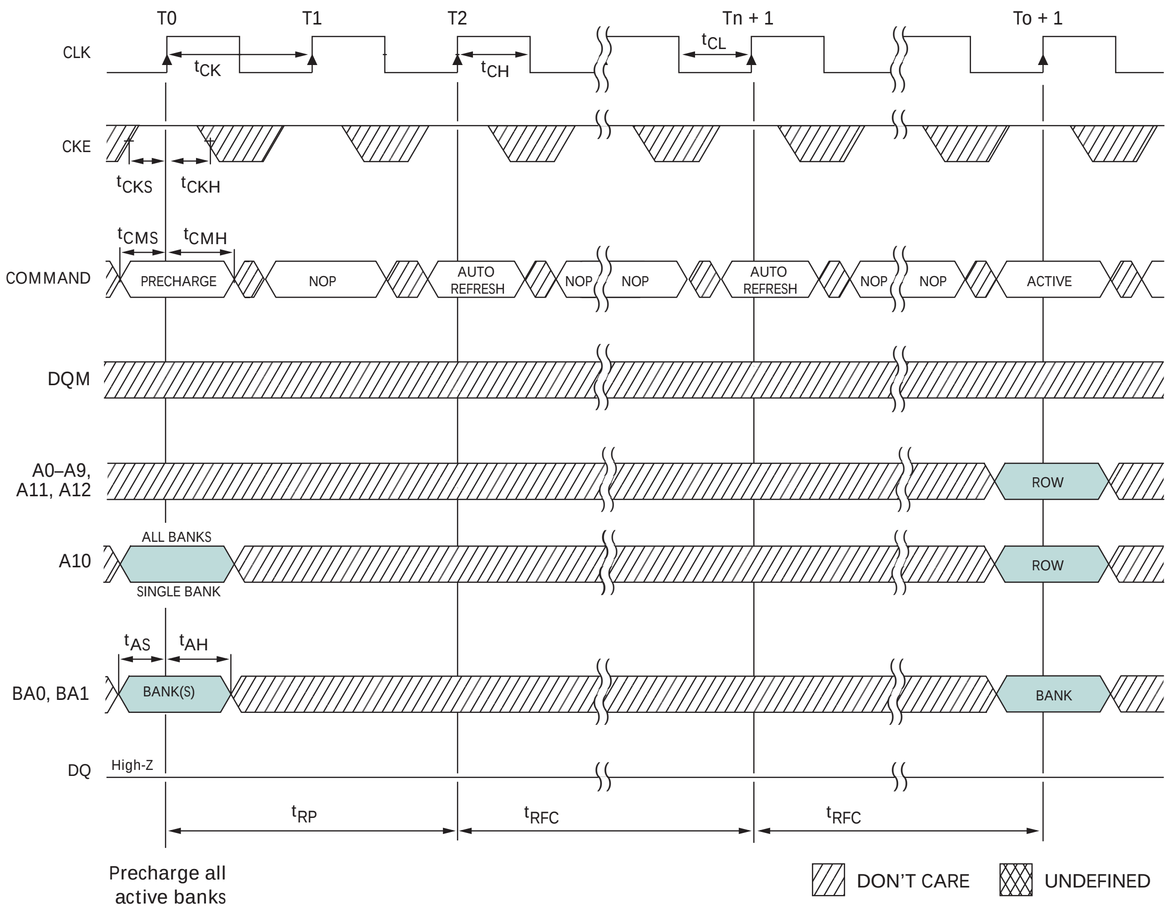
Notes: 1. Violating refresh requirements during power-down may result in a loss of data. See Table 11 on page 47.

Figure 38: Clock Suspend Mode



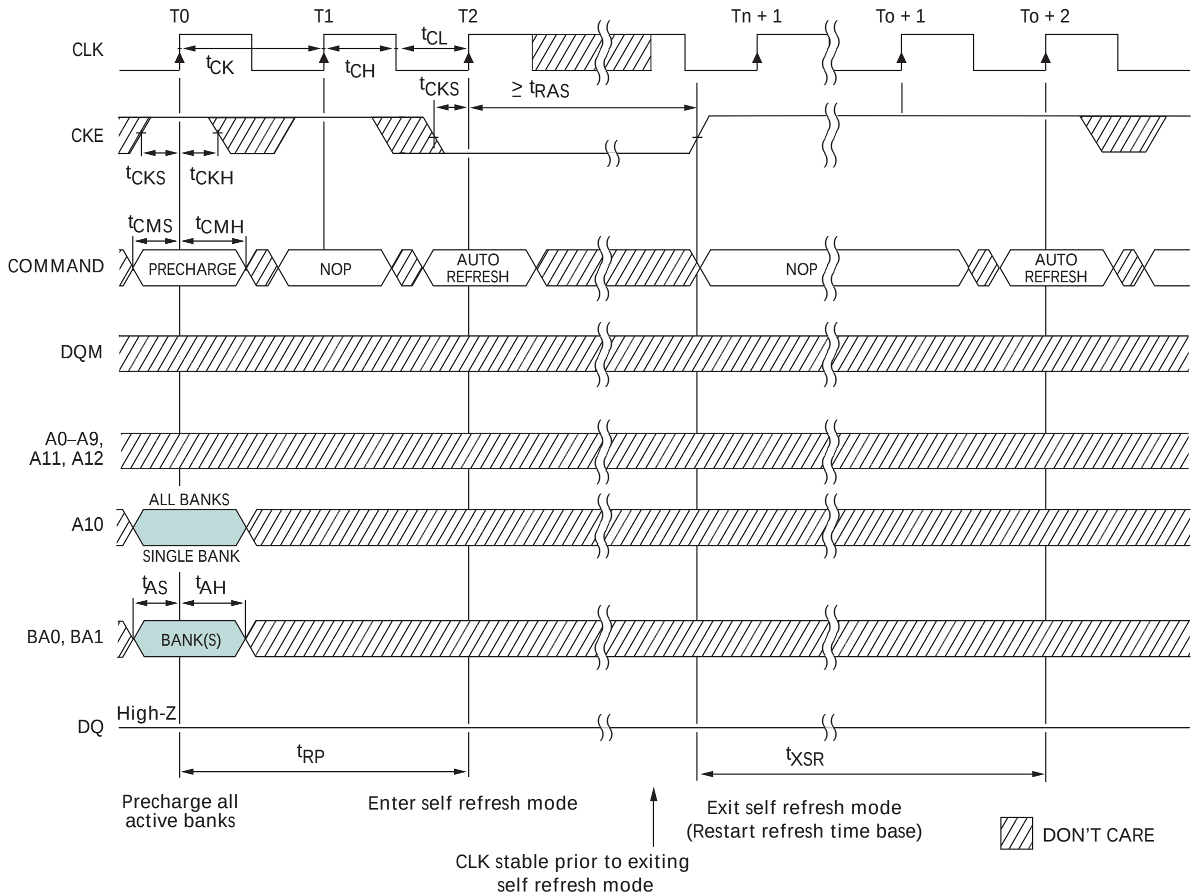
Notes: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.
2. A9 and A11 = "Don't Care." See Table 11 on page 47.

Figure 39: Auto Refresh Mode



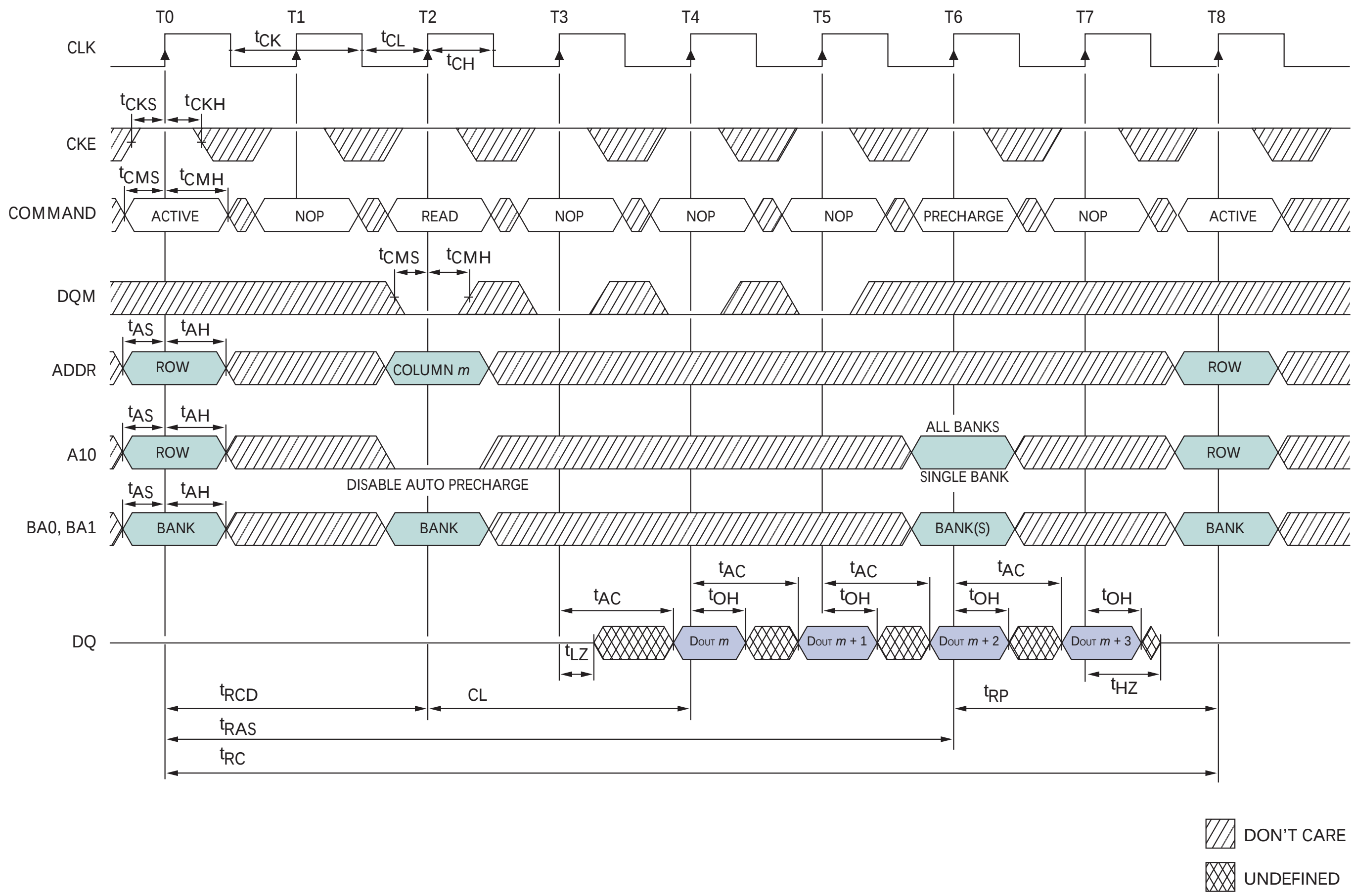
Notes: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required. See Table 11 on page 47.

Figure 40: Self Refresh Mode



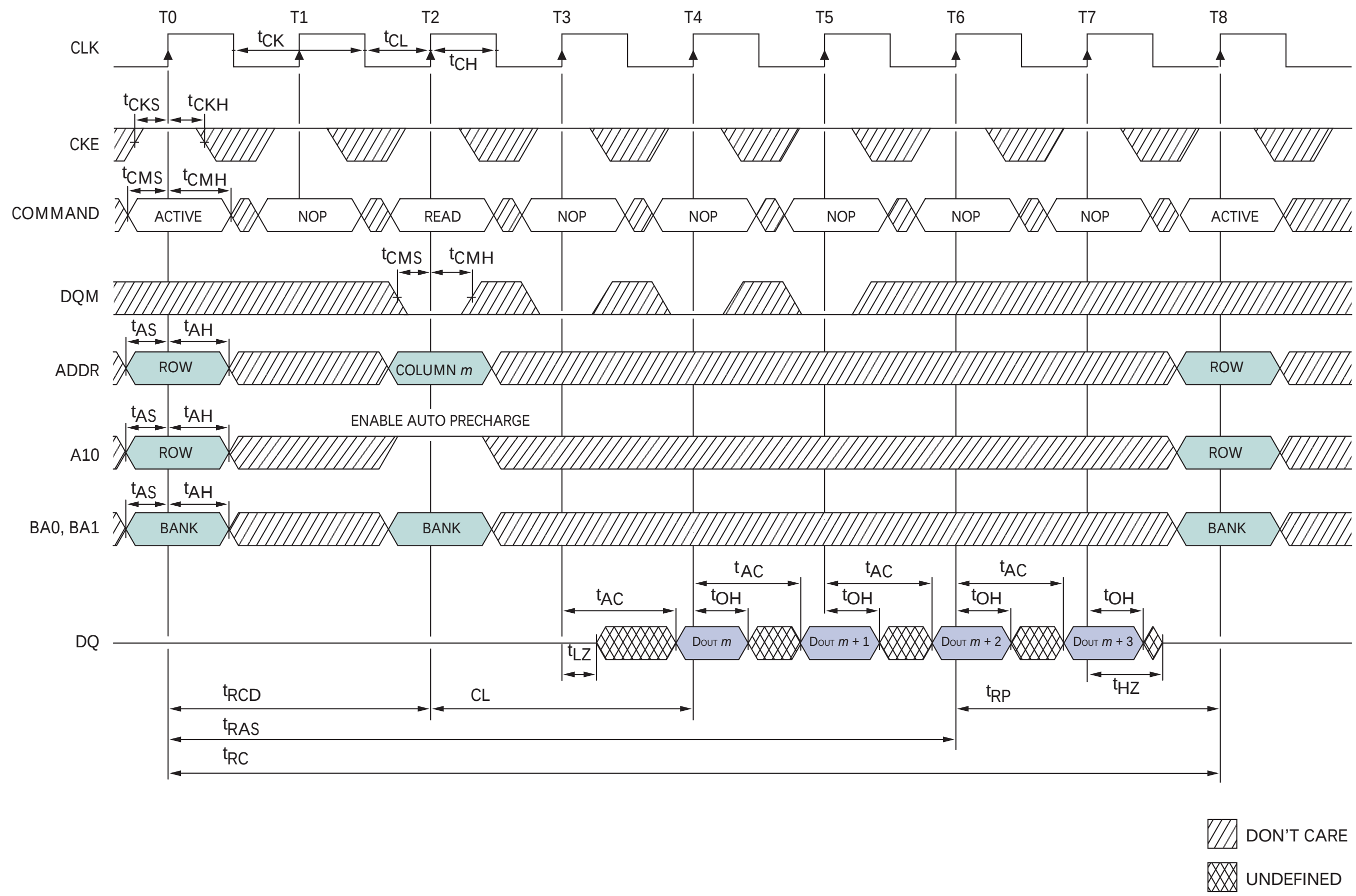
Notes: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required. See Table 11 on page 47.

Figure 41: READ – Without Auto Precharge



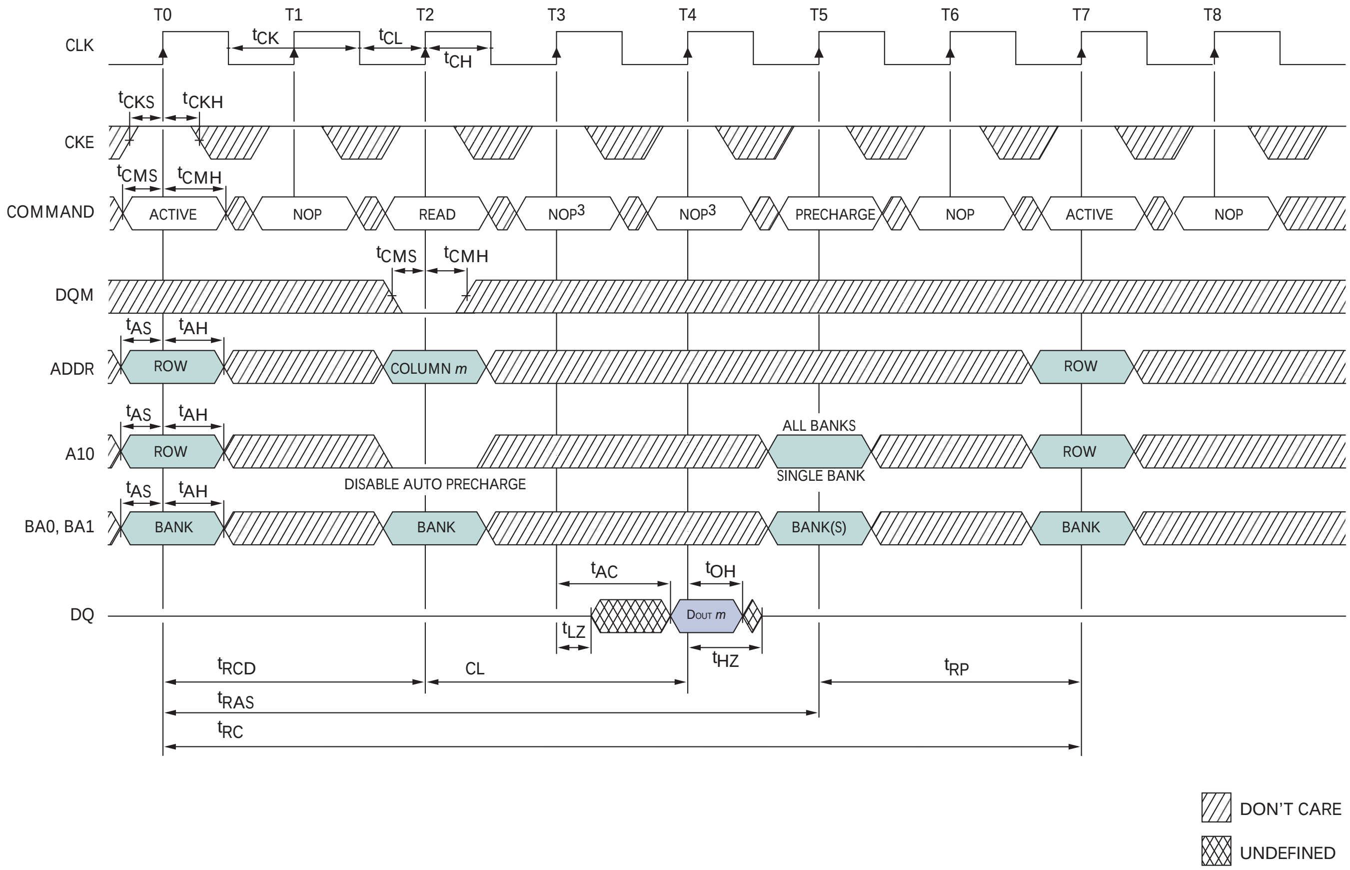
Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.

Figure 42: READ – With Auto Precharge



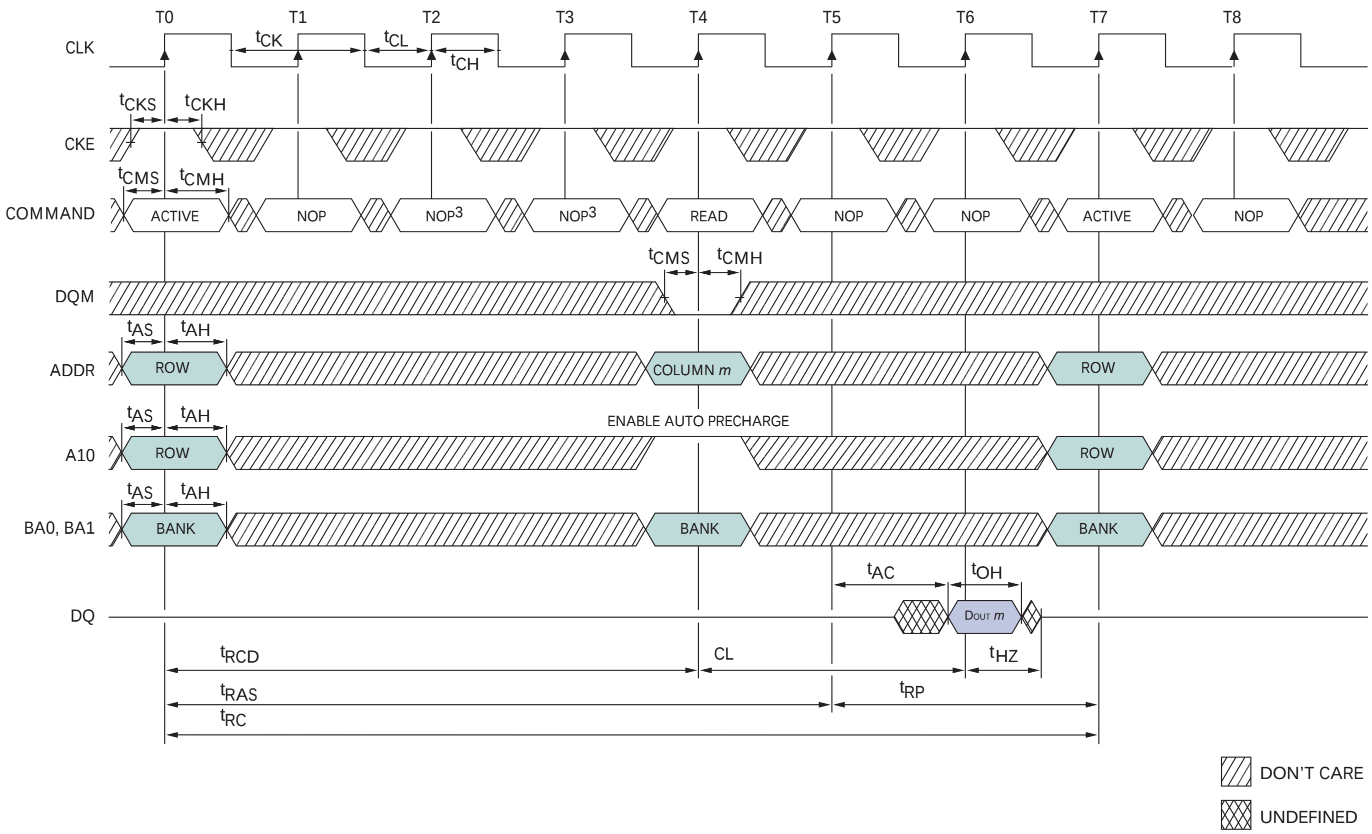
Notes: 1. For this example, BL = 4, CL = 2.

Figure 43: Single READ – Without Auto Precharge



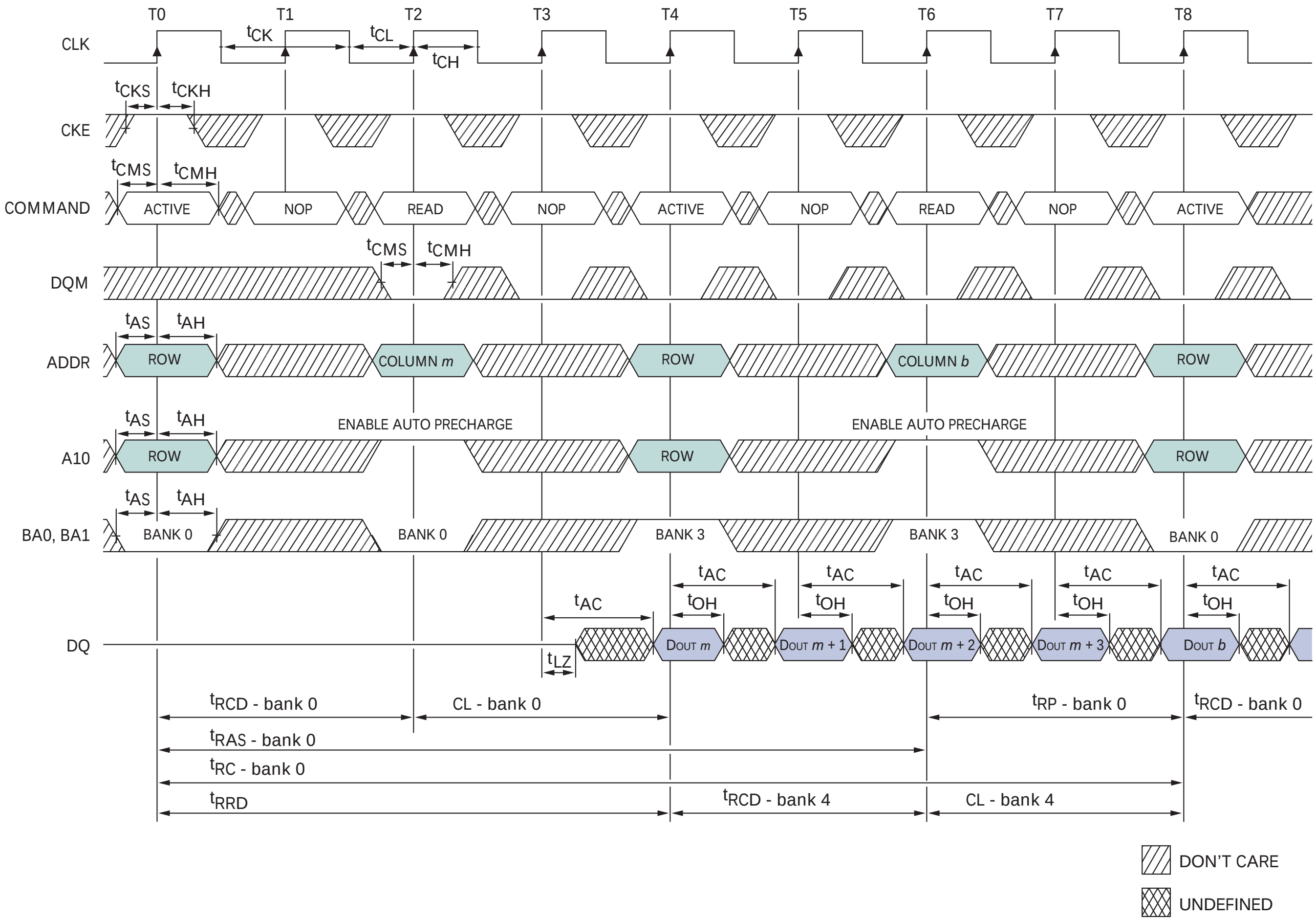
Notes: 1. For this example, BL = 1, CL = 2, and the READ burst is followed by a manual PRECHARGE.

Figure 44: Single READ – With Auto Precharge



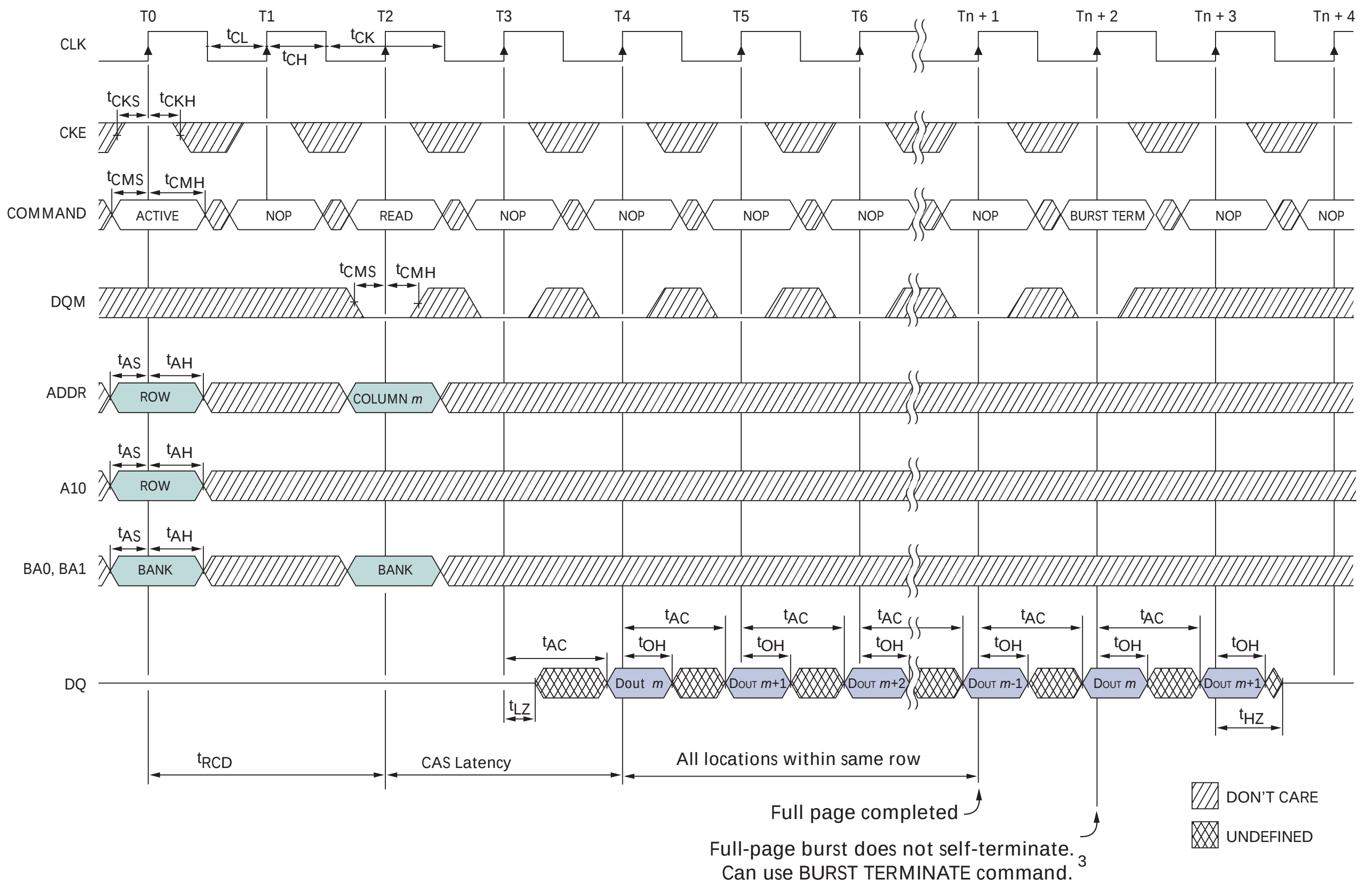
Notes: 1. For this example, BL = 1, CL = 2, and the READ burst is followed by an auto precharge.

Figure 45: Alternating Bank Read Accesses



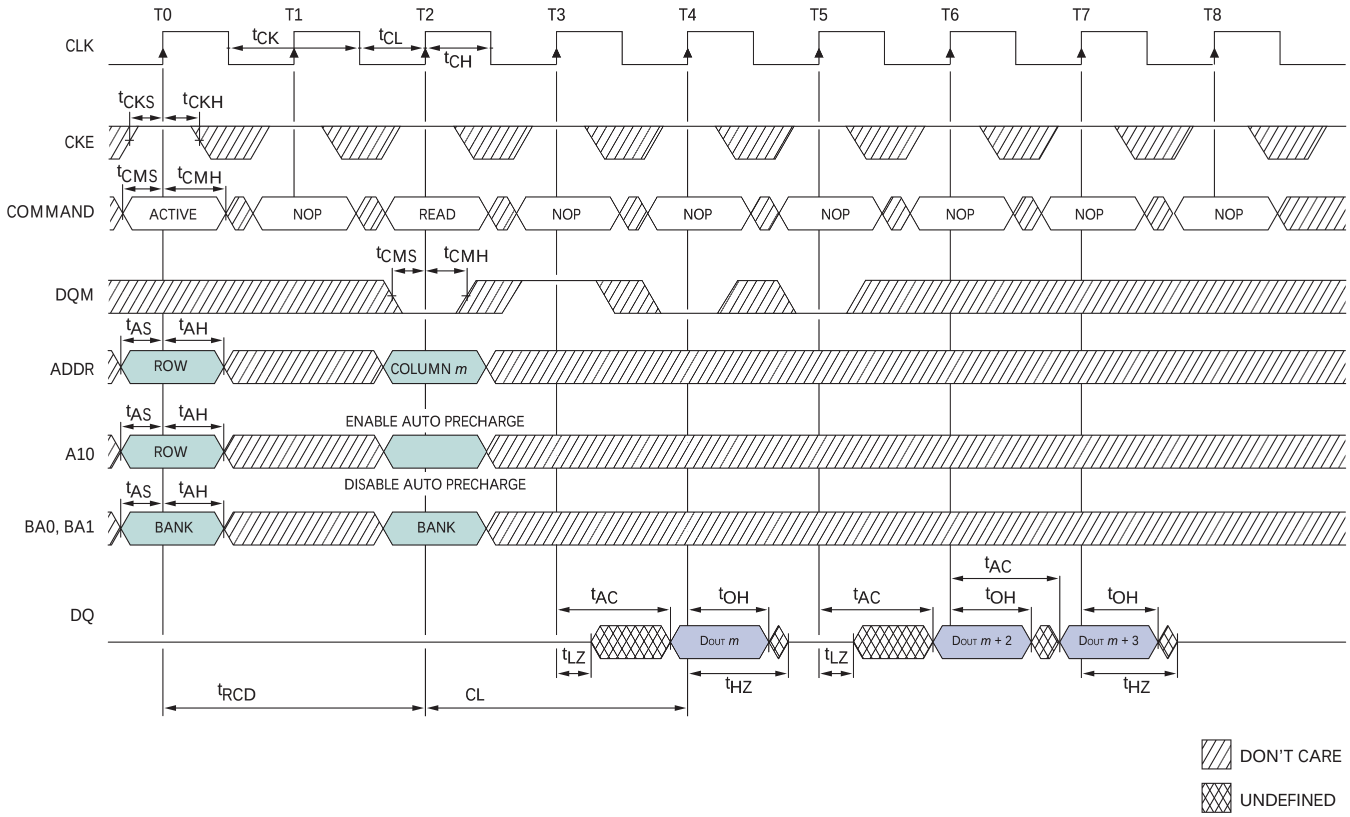
Notes: 1. For this example, BL = 4, CL = 2.

Figure 46: READ – Continuous-Page Burst



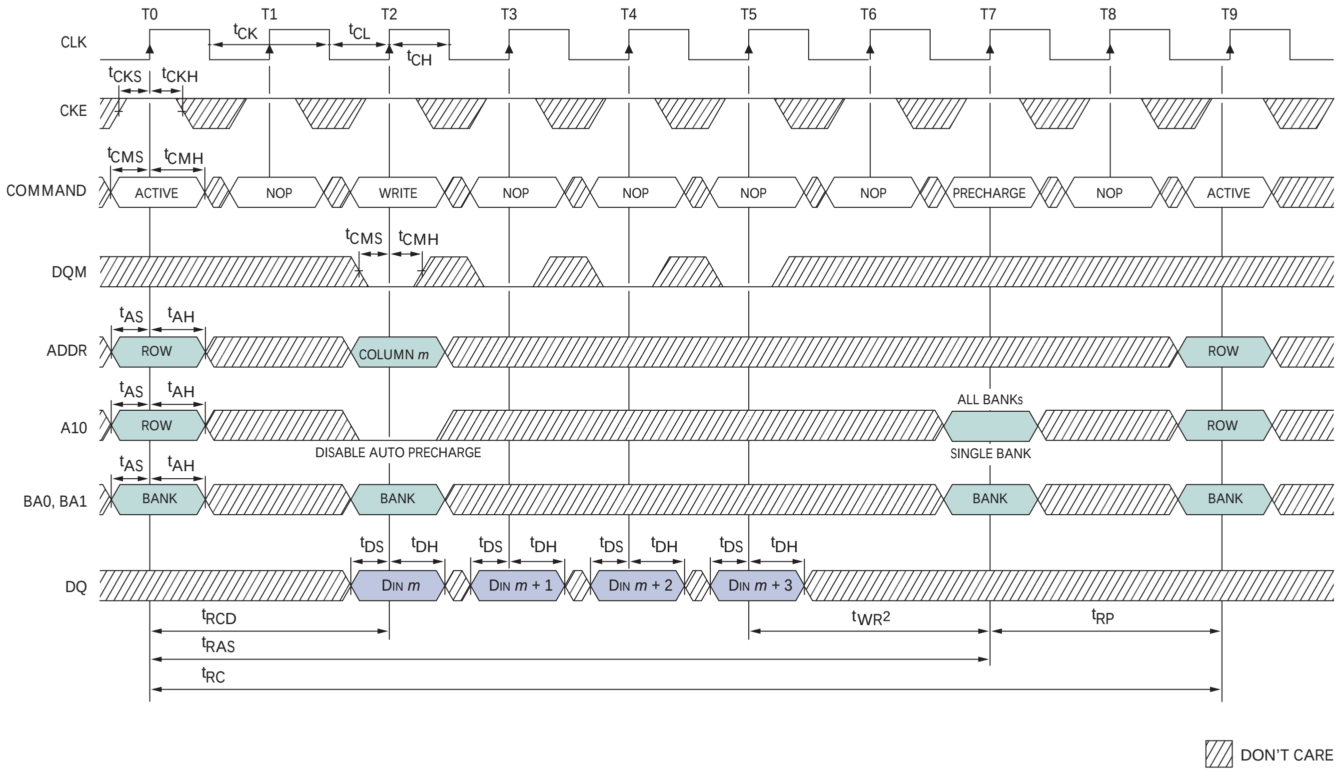
Notes: 1. For this example, CL = 2.

Figure 47: READ – DQM Operation



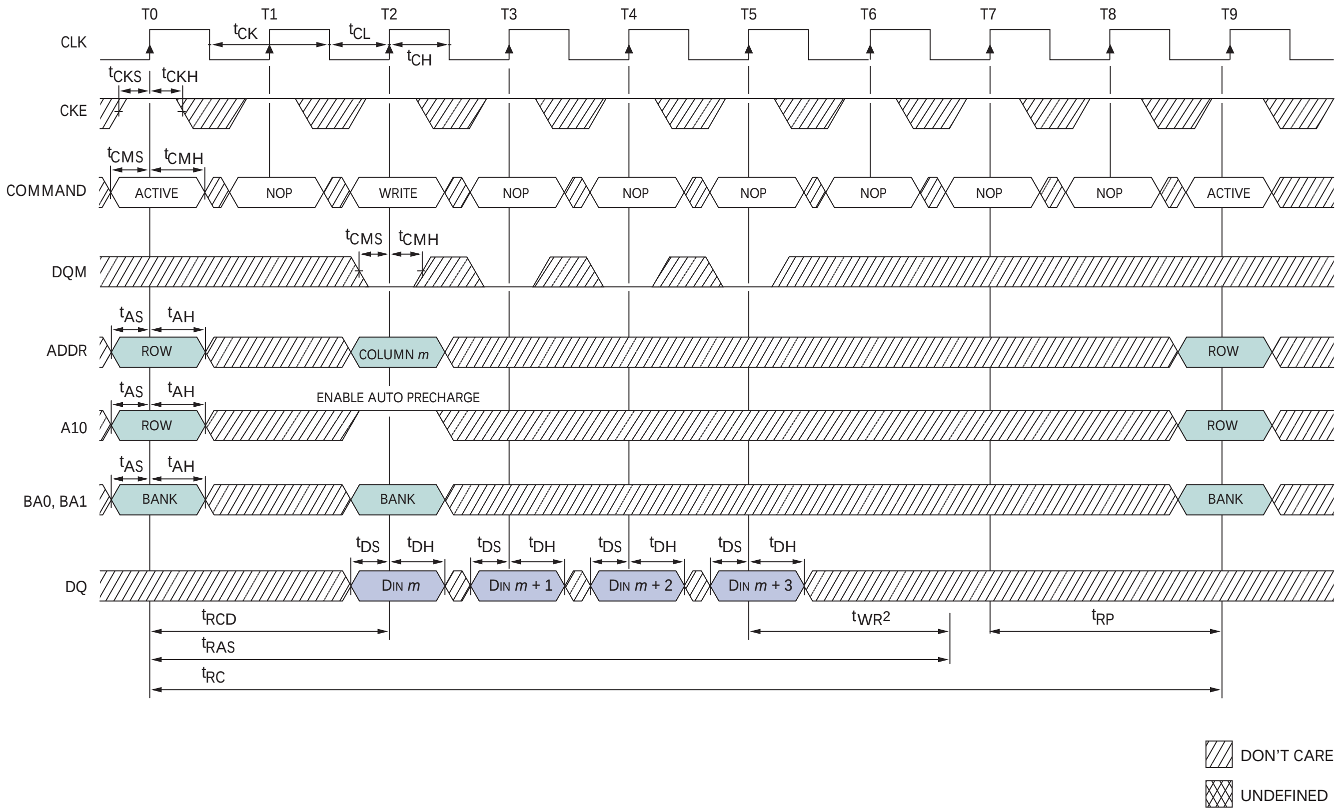
Notes: 1. For this example, CL = 2.

Figure 48: WRITE – Without Auto Precharge



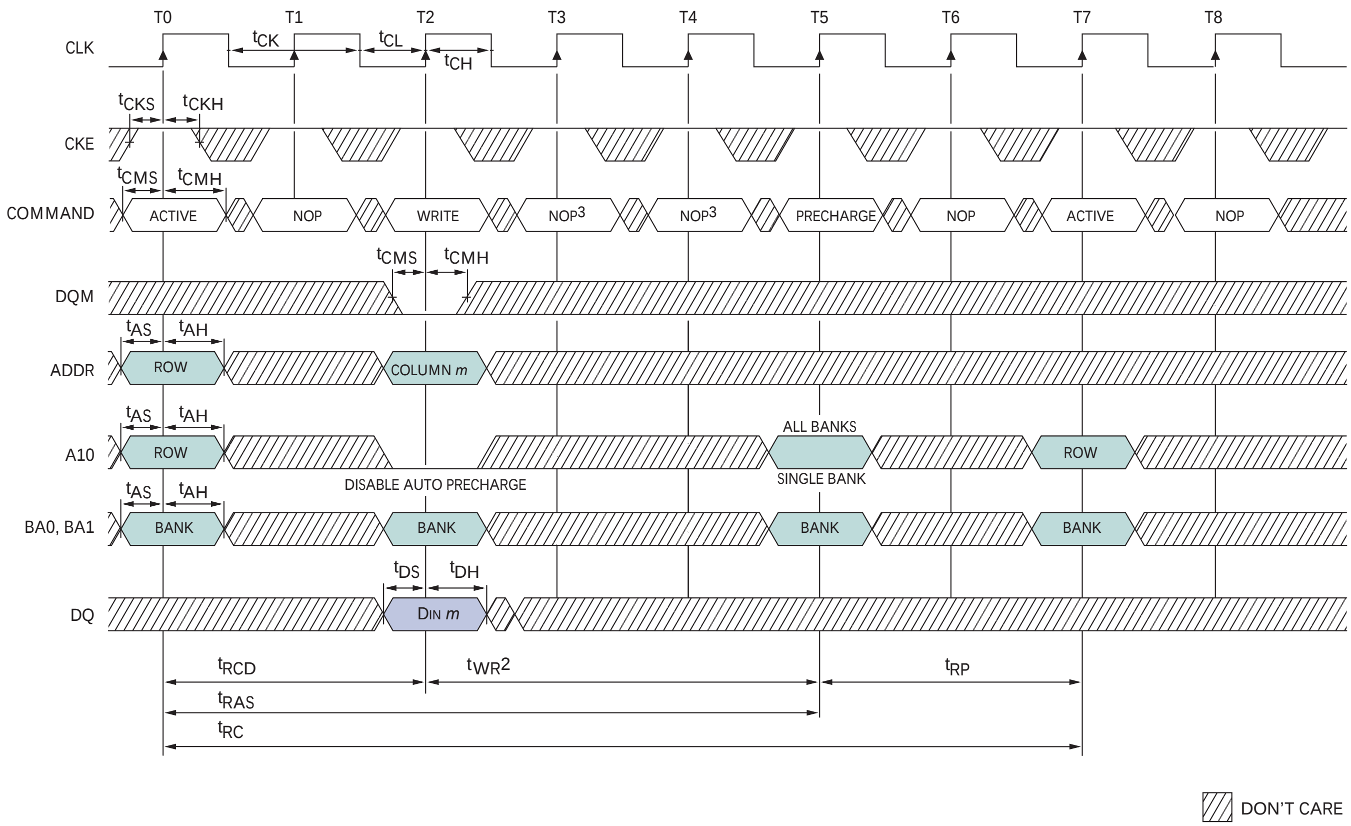
Notes:
1. For this example, BL = 1, and the WRITE burst is followed by an auto precharge.
2. 15ns is required between <DIN m + 3> and the PRECHARGE command, regardless of frequency.

Figure 49: WRITE – With Auto Precharge



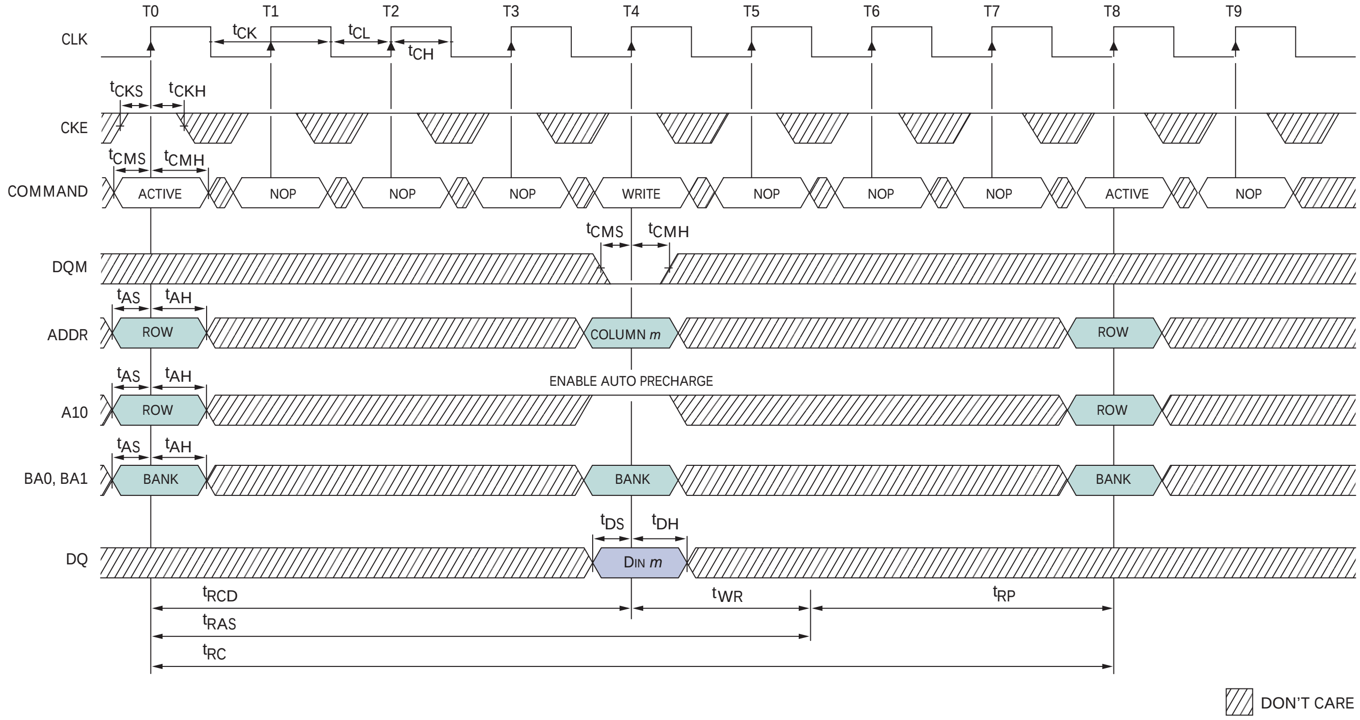
Notes: 1. For this example, BL = 4.
2. There must be one ^{t}CK during the ^{t}WR time for WRITE auto precharge.

Figure 50: Single WRITE – Without Auto Precharge



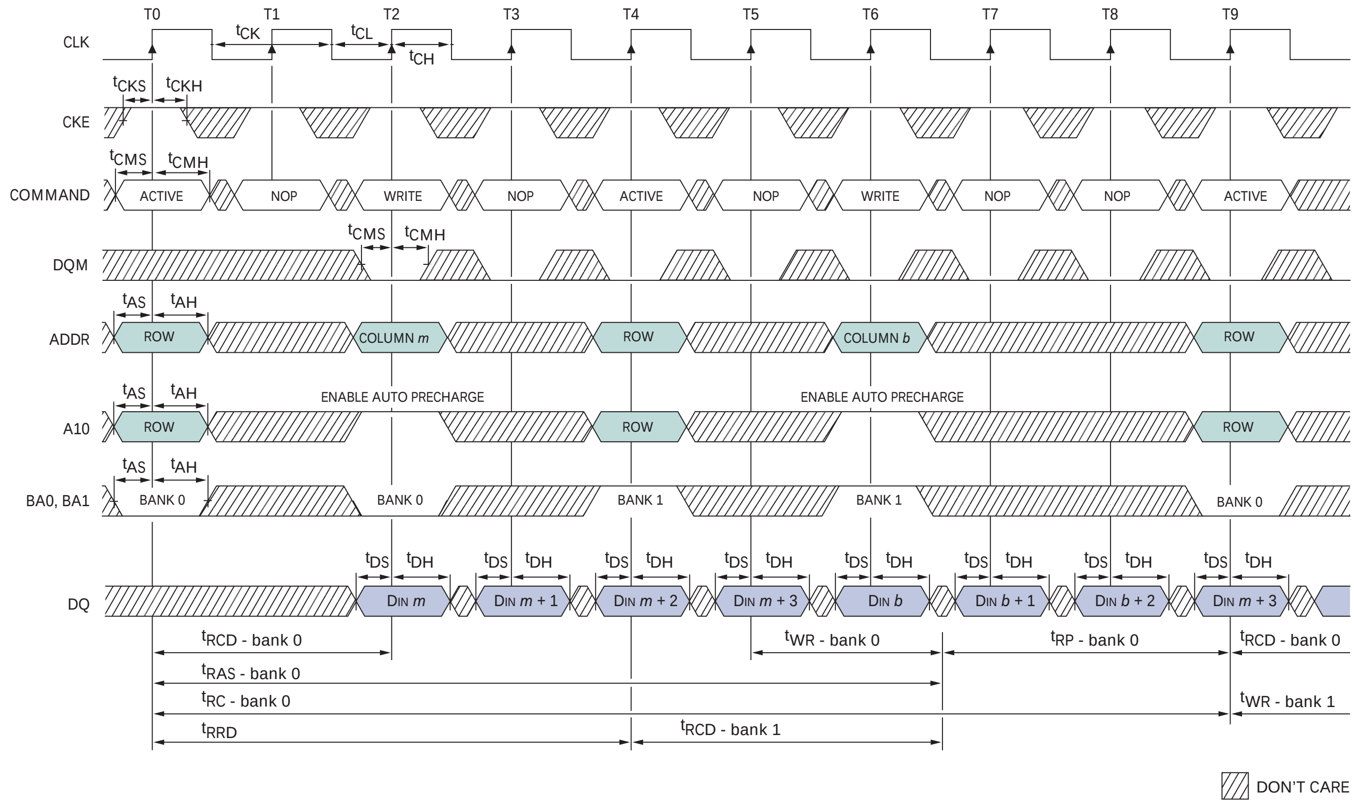
Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE.
2. 15ns is required between <DIN m> and the PRECHARGE command, regardless of frequency.
3. PRECHARGE command not allowed or ^{t}RAS would be violated.

Figure 51: Single WRITE – With Auto Precharge



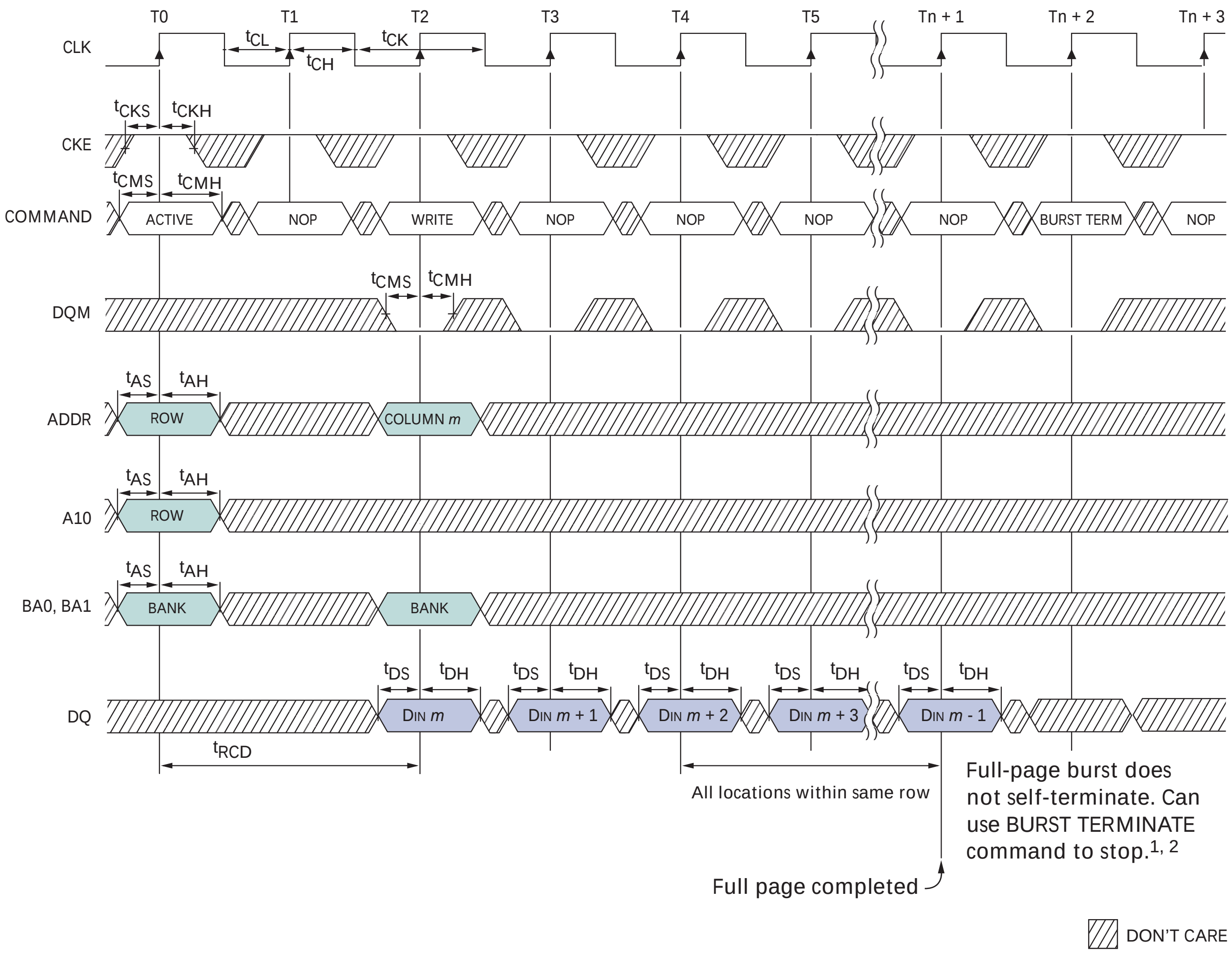
Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE.
2. There must be one ᵗCK during the ᵗWR time for WRITE auto precharge.

Figure 52: Alternating Bank Write Accesses



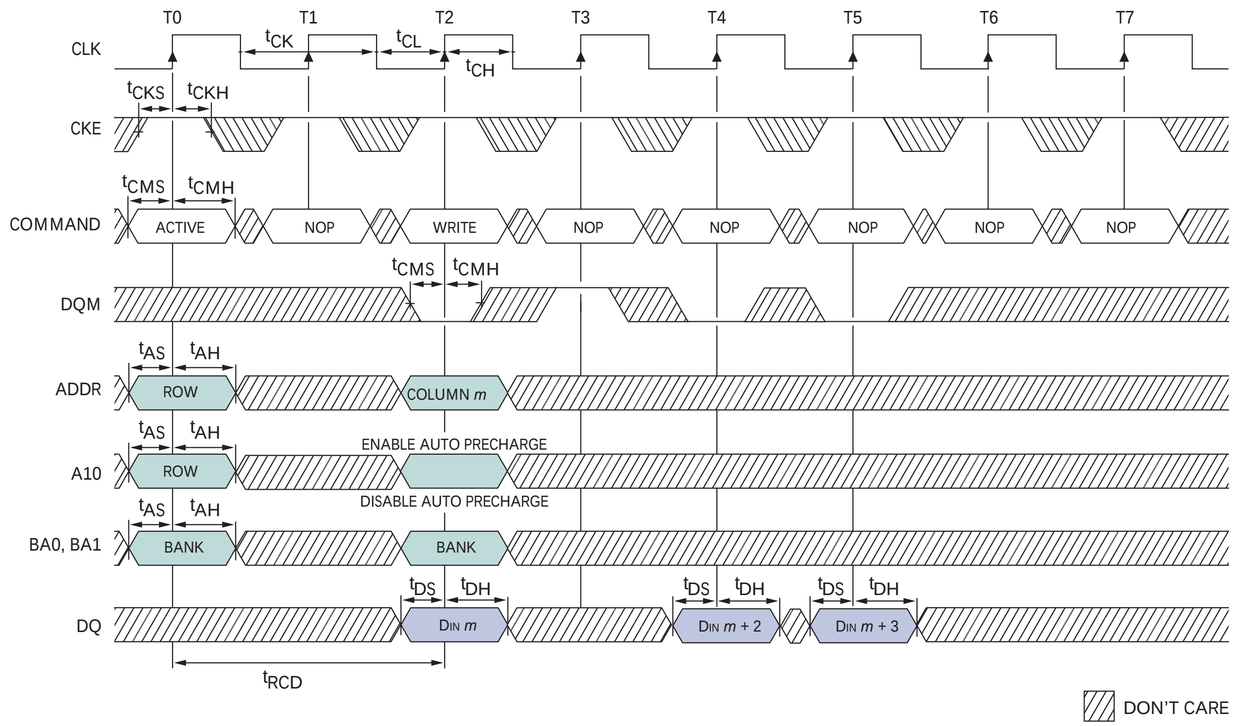
Notes: 1. For this example, BL = 4.

Figure 53: WRITE – Continuous-Page Burst



Notes:
1. ^{t}WR must be satisfied prior to PRECHARGE command.
2. Page left open; no ^{t}RP.

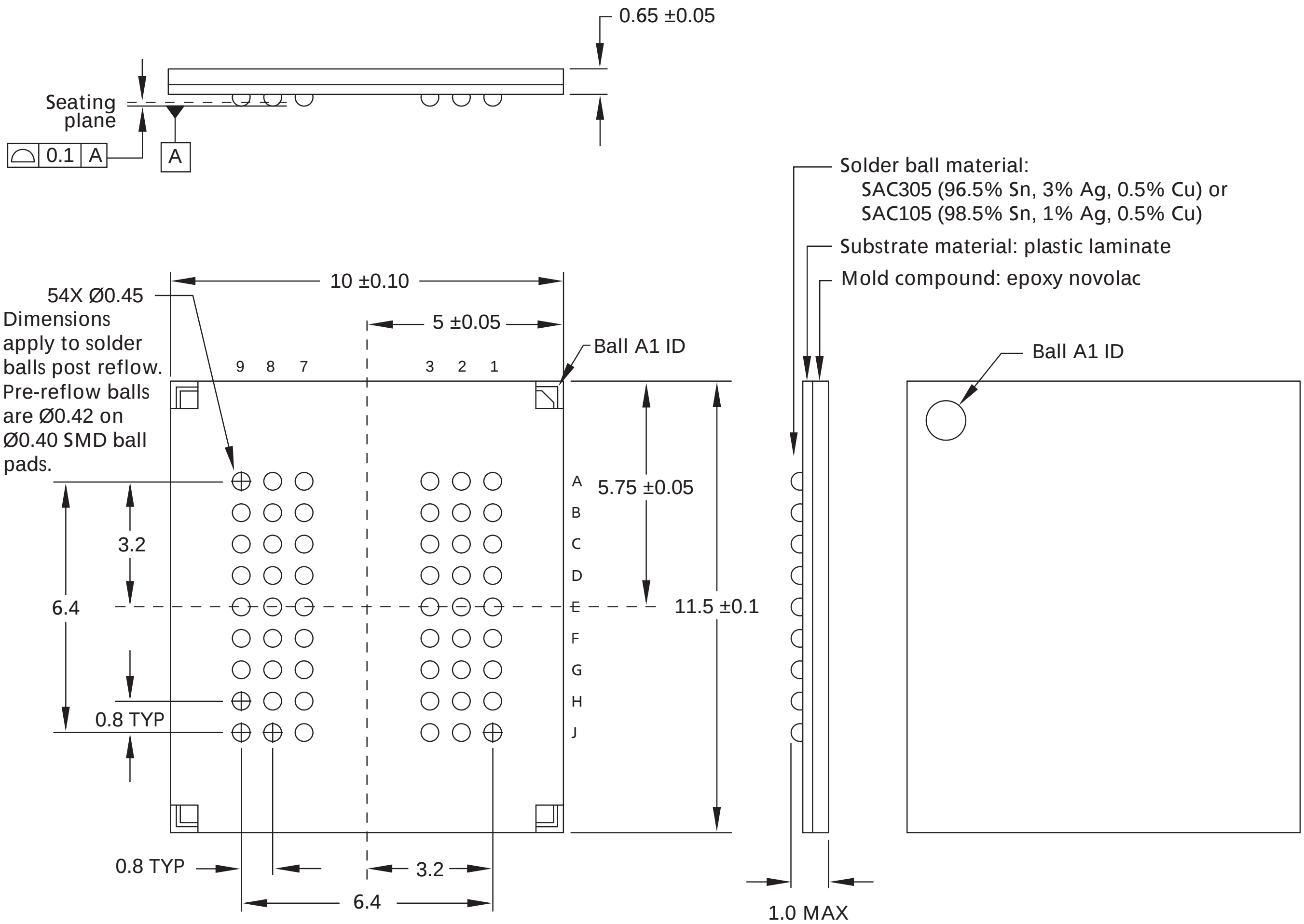
Figure 54: WRITE – DQM Operation



Notes: 1. For this example, BL = 4.

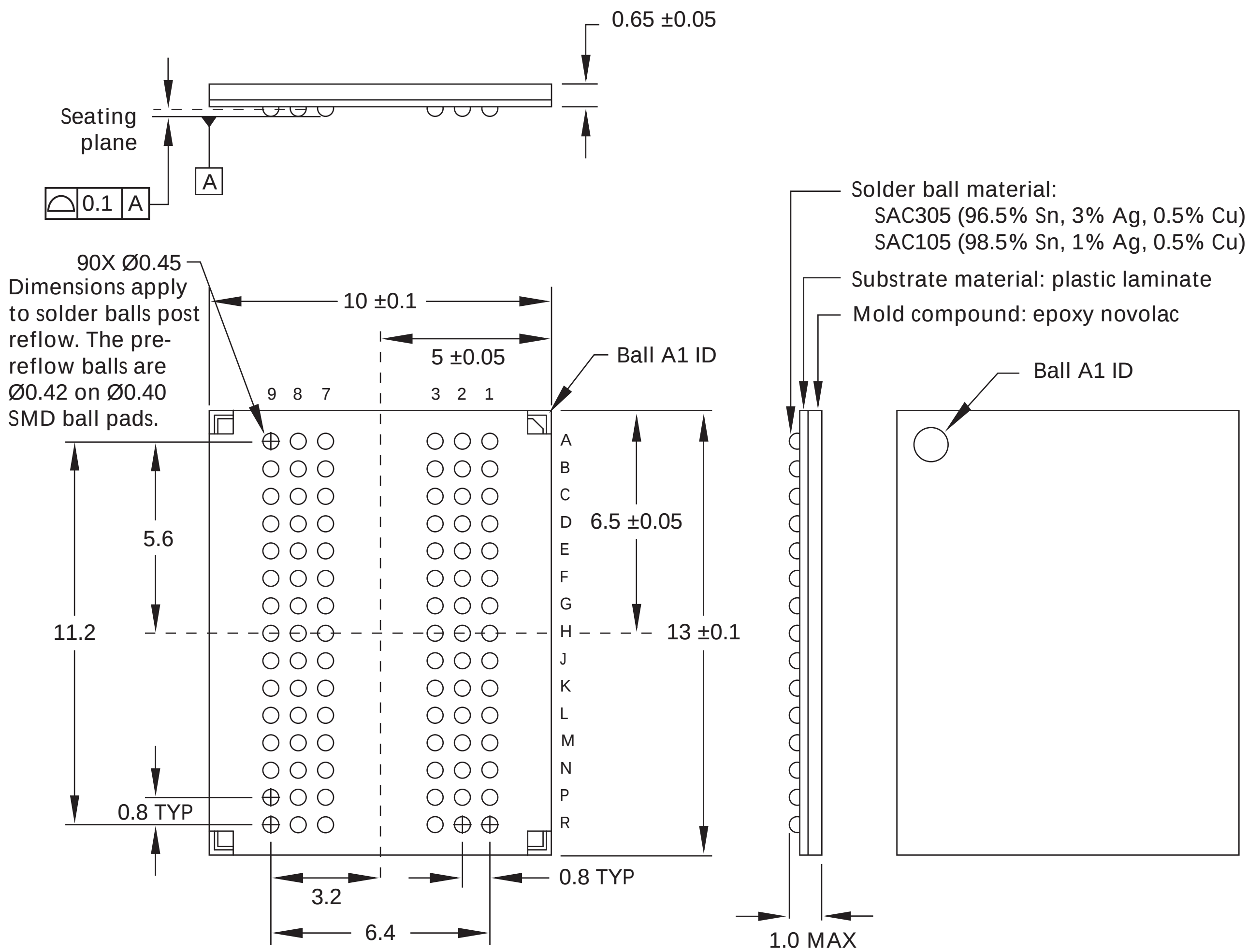
Package Dimensions

Figure 55: 54-Ball VFBGA (10mm x 11.5mm)



Notes: 1. All dimensions are in millimeters.
2. Green packaging composition is available upon request.

Figure 56: 90-Ball VFBGA (10mm x 13mm)



Notes:
1. All dimensions are in millimeters.
2. Green packaging composition is available upon request.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992